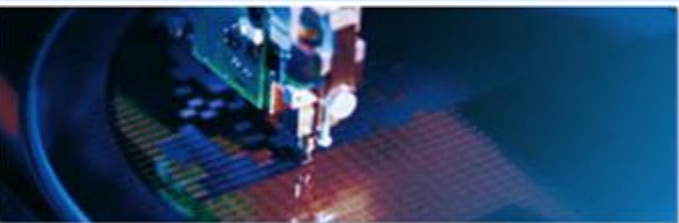
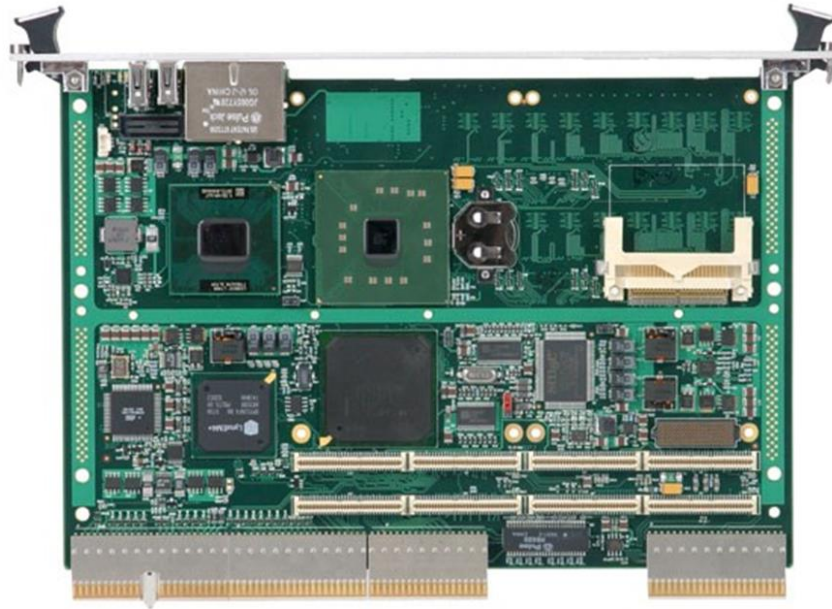


USER MANUAL



CPU-31-12 (CPD/CRD) CompactPCI Intel® Core™ Duo Single Board Computer

CPDMAN202

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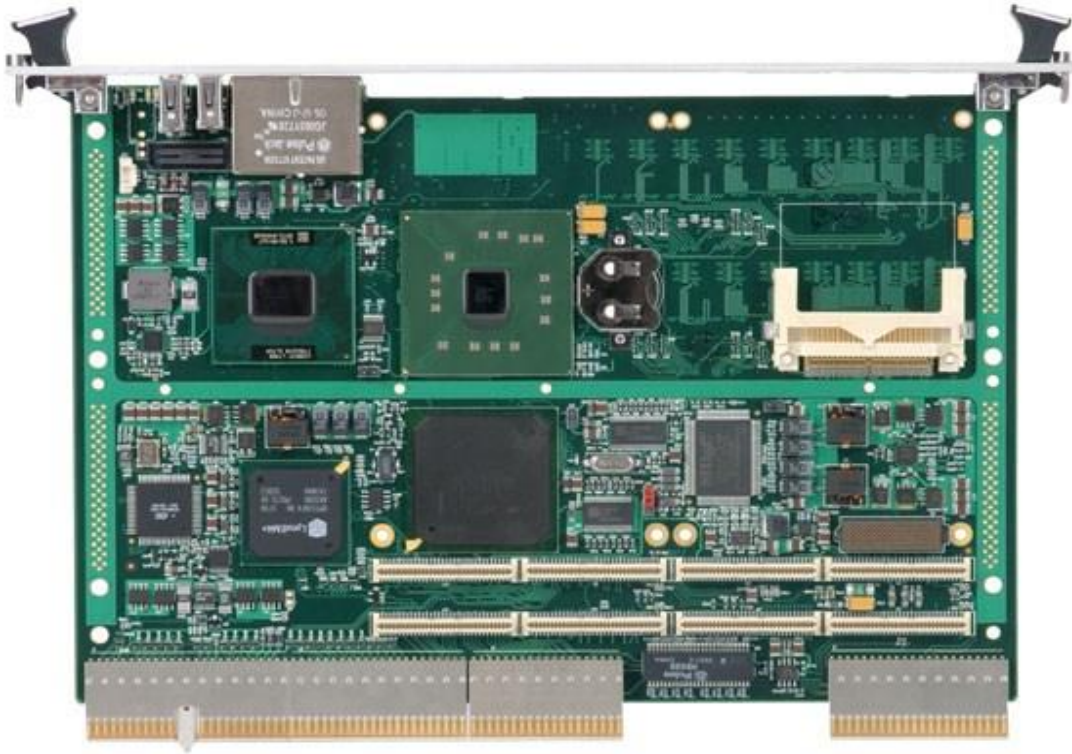
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1. Features

The Dynatem CPU-31-12 is a single-slot 6U CompactPCI Single Board Computer (SBC). The CPU-31-12 offers full PC performance with a Core2 Duo processor. The CPU-31-12 is available in two versions: the lower cost CPU-31-12 for standard industrial applications and the 1101.2 compliant, conduction-cooled CRD with wedgelocks, stiffener bar, and a full board heatsink for rugged applications. When referring to attributes of both versions, we will use the common name CPU-31-12. The CPU-31-12 employs Intel's embedded technology to assure long-term availability.



Features of the CPU-31-12 include:

- Supports either a 1.66 GHz Intel® Core™ Duo processor with 2 MB of L2 cache or a 1.50 GHz Intel® Core™ 2 Duo processor with 4 MB of L2 cache
- Single-slot CompactPCI operation with on-board CompactFlash disk for bootable mass storage and front panel connectors for two USB 2.0 ports, two Fast Ethernet ports, and openings for two PMC I/O bezels
- Two PICMG 2.16 compliant Gbit Ethernet ports and I/O from PMC site #2 are routed to the J3 connector
- Two Serial ATA ports, VGA graphics, two RS232 COM ports, two USB ports, and PS/2 mouse and keyboard ports are routed to J5
- Optionally either PMC/XMC site #1 I/O or an IDE port and two RS232 COM ports are routed to the backplane connector J5

Chapter 1 – Features

- The Intel® E7520 Memory Controller Hub (MCH) and Intel® 6300ESB I/O Controller Hub (ICH) provide high-speed memory control, 16 lanes of PCI Express I/O, integrated I/O like Serial ATA, USB 2.0, IDE supporting Ultra 100 DMA Mode for transfers up to 88.88 MB/sec, and 64 bit PCI-X bus transfers at 66 MHz
- Silicon Motion's SM712 VGA Controller
- Two Intel 82571EB Ethernet Controllers with a x4 PCI Express interface, each offering two 1 Gb Ethernet support; two ports are routed to J3 in compliance with PICMG 2.16 for backplane fabric switching while the other two are routed to the front panel
- 2 GB of DDR2-400 DRAM provided on-board (4 GB of DRAM is supported using TwinDie chips)
- PLX PCI6540 dual mode Universal asynchronous 64 bit 66 MHz PCI-X to PCI-X bridge lets the CPU-31-12 act as a peripheral card or system slot module
- PCI Mezzanine Card (PMC) expansion supports 64 bits @ up to 66 MHz
- A second PCI Mezzanine Card (PMC) expansion supports 64 bits @ up to 66 MHz and can also support an MC module with up to x8 PCI Express
- Secondary IDE port for CompactFlash on-board for flash-based or mechanical mass storage for 1 slot booting
- General Software's Version 6.0 flash-based system BIOS
- PXE for diskless booting over Ethernet
- Programmable watchdog timer for system recovery and a CPLD for LED control, Geographical Addressing, and Built-In Test (BIT) status and control
- Operating System (OS) and driver support, including Windows NT, Embedded NT, XP, QNX, VxWorks, Linux, Solaris, and pSOS+.

2. Related Documents

Listed below are documents that describe the Pentium processor and chipset, and the peripheral components used on the CPU-31-12. Either download from the Internet or contact your local distributor for copies of these documents.

The CPU-31-12 uses the L2400 Low Voltage Core Duo. For information on this processor, go to:

<http://developer.intel.com/design/mobile/core/duodocumentation.htm>

For the ICH component in the 6300ESBchipset get the *Intel® 6300ESB I/O Controller Hub Datasheet*. It is document number 300641-002.

<ftp://download.intel.com/design/intarch/datashts/30064102.pdf>

For information on the E7520 MCH component in the chipset, please go to:

http://www.intel.com/design/chipsets/embedded/e7520_7320.htm

For data sheets on I/O controllers:

- *82571EB Fast Ethernet PCI Controller*
<http://www.intel.com/design/network/products/lan/controllers/82571eb.htm>
- *CompactPCI Interface Components Manual*
Tundra Semiconductor Corporation; Universe IID revisions are found at www.tundra.com

The following documents provide information on the PC architecture and I/O:

- *PCI Local Bus Specification, Revision 2.2* <http://www.pcisig.com/specifications/>
- *PCI-X Specification, Revision 1.0A* <http://www.pcisig.com/specifications/>
- *System Management Bus Specification (SMBus), Revision 1.1* <http://www.smbus.org/specs/>
- *Universal Serial Bus Specification* <http://www.usb.org/developers>

The following documents cover topics relevant to the CompactPCI and can be purchased through VITA:

- IEEE Std 1014-1987, *IEEE Standard for a Versatile Backplane Bus: CompactPCI*
The Institute of Electrical and Electronic Engineers
345 East 47th Street
New York, NY 10017
(800) 678-4333

Chapter 2 – Related Documents

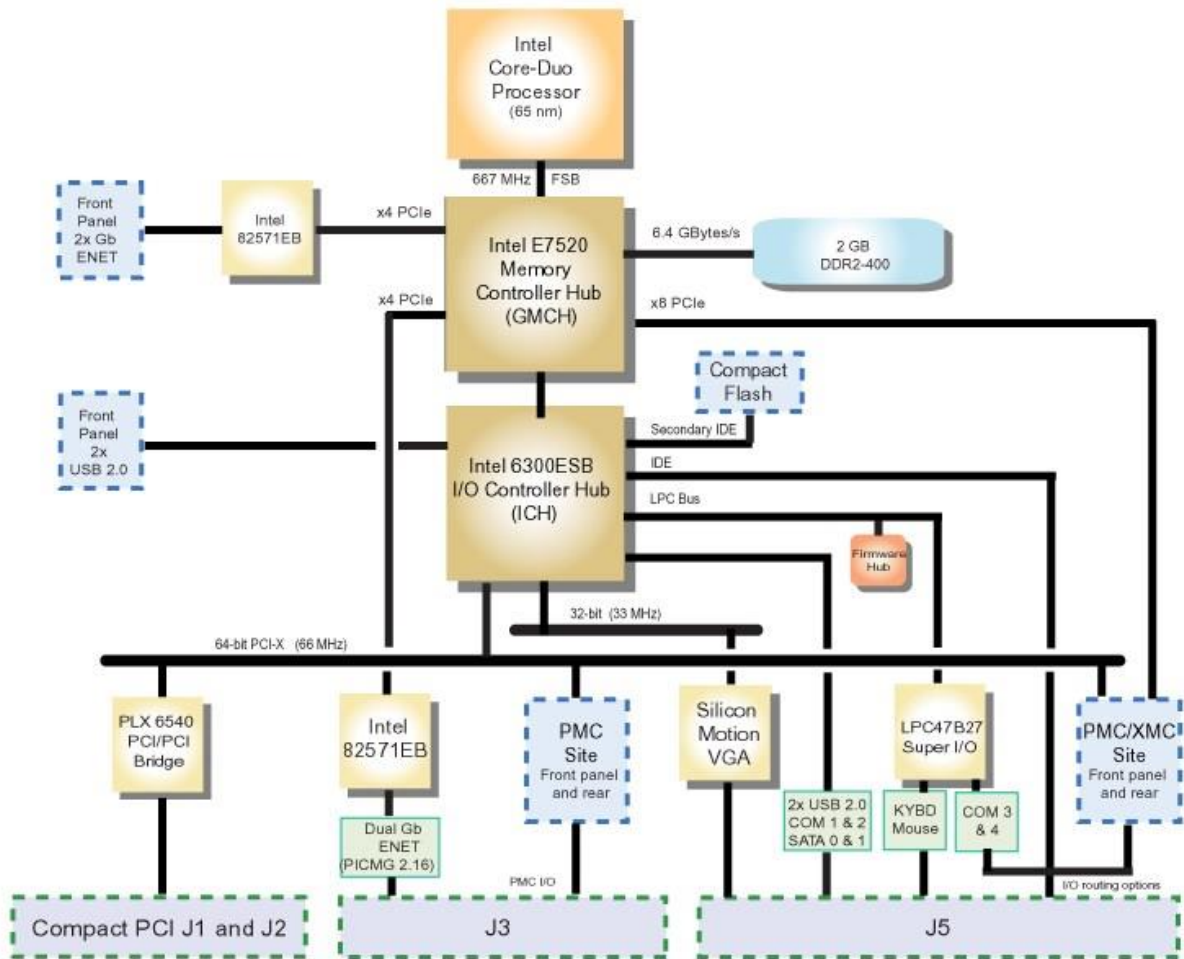
The following documents are the current draft standards for the PCI Mezzanine Card (PMC) and XMC cards:

- IEEE Draft Std P1386/2.0, *Draft Standard for a Common Mezzanine Card Family: CMC*
The Institute of Electrical and Electronic Engineers
345 East 47th Street
New York, NY 10017
(800) 678-4333
- IEEE Draft Std P1386.1/2.0, *Draft Standard Physical and Environmental Layers for PCI Mezzanine Cards: PMC*
The Institute of Electrical and Electronic Engineers
345 East 47th Street
New York, NY 10017
(800) 678-4333
- VITA 42.0, XMC Switched Mezzanine Card Auxiliary Standard
VITA
10229 North Scottsdale Road, Suite B
Scottsdale, AZ 85253
(480) 951-8866

3. Hardware Description

3.1 Overview

The block diagram of the CPU-31-12 is shown below. The sections that follow describe the major functional blocks of the CPU-31-12.



3.2 Processor

The CPU-31-12 supports either a Core Duo processor at 1.66 GHz with 2 GB of L2 cache or a 1.50 GHz Core2 Duo with 4 MB of L2 cache. The Intel Core Duo processor with 2 MB of L2 cache is the first dual core processor available for mobile and embedded applications. Features include:

- 667 MHz front side bus (limited by the E7520 FSB).
- On-die, primary 32-KB instruction cache and 32-KB write-back data cache.

- Second-generation Streaming SIMD Extensions 2 (SSE2) and streaming SIMD Extensions 3 (SSE3)
- Supports Intel® Architecture and Dynamic Execution.

For further information on the Core Duo processor available from Intel Corporation, search at:

<http://developer.intel.com/design/mobile/core/duodocumentation.htm>

The Intel® Core™ Duo processor was designed to deliver high, dual processor high performance with low power consumption. With its 65 nm processing technology and 2 MB of L2 advanced transfer cache, the Core Duo offers more performance per Watt. The Thermal Design Power (TDP) is 15 W. Advanced power management included Enhanced Intel SpeedStep Technology are supported. SpeedStep enables clock and core voltage throttling based on temperature or processor loading.

The processor's 667 MHz Front Side Bus utilizes a split-transaction, deferred reply protocol. The FSB uses a Source-Synchronous Transfer (SST) of address and data to improve performance by transferring data four times per bus clock. The address bus can deliver addresses twice per clock cycle. Together, the 4X data bus and 2X address bus provide a data bus bandwidth of up to 5.33 GB/second.

3.3 Chipset

The Intel® E7520 Memory Controller Hub (MCH) and Intel® 6300ESB I/O Controller Hub (ICH) chipset provide memory control, mass storage and basic I/O, and standard PC system resources including the real time clock, NVRAM, timers, thermal management, and interrupt management. Also, the MCH provides 24 lanes of PCI Express expansion (16 of which are implemented on the CPU-31-12) for high-speed expansion through the two dual 1000BaseTX controller chips and the XMC site.. The ICH supports a 32 bit @ 33 MHz PCI bus, to support the Universe CompactPCI interface controller and the Silicon Motion SM712 graphics chip, and a 64 bit @ 66 MHz PCI-X bus for user I/O expansion through the two PMC sites. The ICH also provides a Low Pin Count (LPC) interface for the BIOS flash chip and for Super I/O and an SMBus interface for on-board resources like the DRAM circuit's SPD PROMs and the thermal monitors.

The MCH supports a base system bus frequency of 200 MHz. The address and request interface is double pumped to 400 MHz while the 64-bit data interface (+ parity) is quad pumped to 800 MHz. This provides a matched system bus address and data bandwidth of 6.4 GB/s. The E7520 (MCH) provides a 400 MHz interface to DDR2 RAM (72 bits wide with ECC). The CPU-31-12 can be populated with one or two banks of DRAM for 1 GB or 2 GB of total memory respectively. Each bank is serviced by a separate channel from the MCH that function in lock-step mode.

Memory controller features include:

- Memory mirroring allows for two copies of all data in the memory subsystem (one on each channel) to be maintained.
- Hardware periodic memory scrubbing, including demand scrub support.
- Retry on uncorrectable memory
- ECC is supported
- DDR2-400 DRAM is supported on-board

The 6300ESB I/O Controller Hub (ICH) provides most of the CPU-31-12's on-board I/O and it's the CPU-31-12's PCI-X expansion bridge. The ICH is designed as a low-power, high-performance I/O hub that features:

- 64-bit @ 66 MHz PCI-X expansion that is used on the CPU-31-12 for the two on-board PMC-X slots.

- Four USB 2.0 compliant ports: two of which are routed to the front panel while the other two are routed to the J5 connector to the backplane.
- Integrated IDE controller supports Ultra 100 DMA Mode Transfers up to 100 MB/sec read cycles and 88.88 MB/sec write cycles for a CompactFlash drive on-board and a primary IDE port that is routed through J5 to the XPDDRIO
- Two Serial ATA ports providing 150 MB/sec data rates are routed through J3
- Standard PC functionality like a battery-backed RTC and 256-bytes of CMOS RAM, Power Management Logic, Interrupt Controller, Watchdog Timer, AC'97 CODEC, Integrated 16550 compatible UART's, and multimedia timers based on the 82C54

For further information, see the documents referenced in Section 2

3.4 DRAM

The CPU-31-12 supports two 72-bit wide, DDR2-400 memory interface channels with a memory bandwidth of 6.4 GB/s with ECC. The CPU-31-12 can be populated to support 1GB or 2GB of DRAM.

3.5 Intel 82571EB Dual Gigabit Ethernet Controller

The CPU-31-12 supports two Intel® 82571EB Gigabit Ethernet Controllers, one provides two PICMG 2.16 compliant Gigabit LAN ports to the backplane while the other provides two that are accessible from the front panel. The 82571EB is a single, compact component with two fully integrated Gigabit Ethernet Media Access Control (MAC) and physical layer (PHY) ports. This device uses the PCI Express* architecture (Rev. 1.0a), and also enables a dual-port Gigabit Ethernet implementation in a very small area, which is useful for embedded designs with critical space constraints. The Intel 82571EB Gigabit Ethernet Controller provides two IEEE 802.3 Ethernet interfaces for 1000BASE-T, 100BASE-TX, and 10BASE-T applications. In addition to managing MAC and PHY Ethernet layer functions, the controller manages PCI Express packet traffic across its transaction, link, and physical/logical layers.

The Intel 82571EB Gigabit Ethernet Controller for PCI Express is designed for high performance and low memory latency. The device is optimized to connect to the E7520 MCH using four PCI Express lanes. Alternatively, the controller can connect to an Input/Output (I/O) Control Hub (ICH) that has a PCI Express interface. Wide internal data paths eliminate performance bottlenecks by efficiently handling large address and data words. Combining a parallel and pipelined logic architecture optimized for Gigabit Ethernet and for independent transmit and receive queues, the controller efficiently handles packets with minimum latency. The controller includes advanced interrupt handling features and uses efficient ring-buffer descriptor data structures, with up to 64 packet descriptors cached on chip. A large 48 KByte per port on-chip packet buffer maintains superior performance. In addition, using hardware acceleration, the controller offloads tasks from the host, such as checksum calculations for transmission control protocol (TCP), user datagram protocol (UDP), and Internet protocol (IP); header and data splitting; and TCP segmentation.

The Intel 82571EB offers the following features:

- 10, 100, and 1000BaseTX support with auto-negotiation
- Uses x4 PCI Express from MCH
- Dual 48 KB configurable RX and TX packet FIFOs
- Built-in Phyceiver
- Serial EEPROM for non-volatile Ethernet address storage

Chapter 3 – Hardware Description

Both 10/100/1000BaseTX ports of one 82571EB device are brought out to the J3 backplane connector in compliance with the PICMG 2.16 specification. PICMG 2.16 permits fabric switching on the backplane where 31.1 compliant SBC's can communicate with each other and with an external network through switch modules that are located at either end of the backplane. Optionally these two 1 Gb Ethernet ports are brought to industry standard RJ-45 connectors on Dynatem's rear I/O plug-in module (XPDDRIO).

The two Ethernet ports provided by the CPU-31-12's 2nd 82571EB are accessible from the front panel.

Technical documents on Intel's 82571EB Dual Gigabit Ethernet Controller are available at:

http://www.intel.com/design/network/products/lan/docs/82571eb_docs.htm

3.6 Silicon Motion SM712 VGA Controller

The Silicon Motion SM712 processor generates VGA graphics which are routed to the J3 backplane connector. A VGA connector is provided by the optional XPDDRIO rear-I/O module.

The SM712's features include:

- Supports both independent displays at 1280x1024, 24bpp, 60Hz in 64-bit, and 1024x768, 24bpp, 60Hz in 32-bit (see mode tables for details).
- Primary display path supports VGA and accelerated modes, video overlay, hardware cursor, hardware icon (128x128), and 24-bit palette gamma correction.

The SM712 offers low power graphics for limited GUI purposes. It attaches to the system via the ICH's 32 bit @ 33 MHz PCI bus.

Silicon Motion SM712 Signal	PCI Bus Connection
Bus	PCI
IDSEL	AD17
REQ#	REQ1#
GNT#	GNT1#
INTR#	INTB#

3.7 PLX PC6540 PCI CompactPCI Backplane Interface

The CPU-31-12 uses the PLX PCI6540 as its PCI-X to PCI-X bridge to the CompactPCI backplane. The PCI6540 shares its primary side with the two PMC sites on the CPU-31-12. Peripheral modules plugged into these PMC sites must support PCI-X transfers or the PCI6540 cannot operate in PCI-X mode.

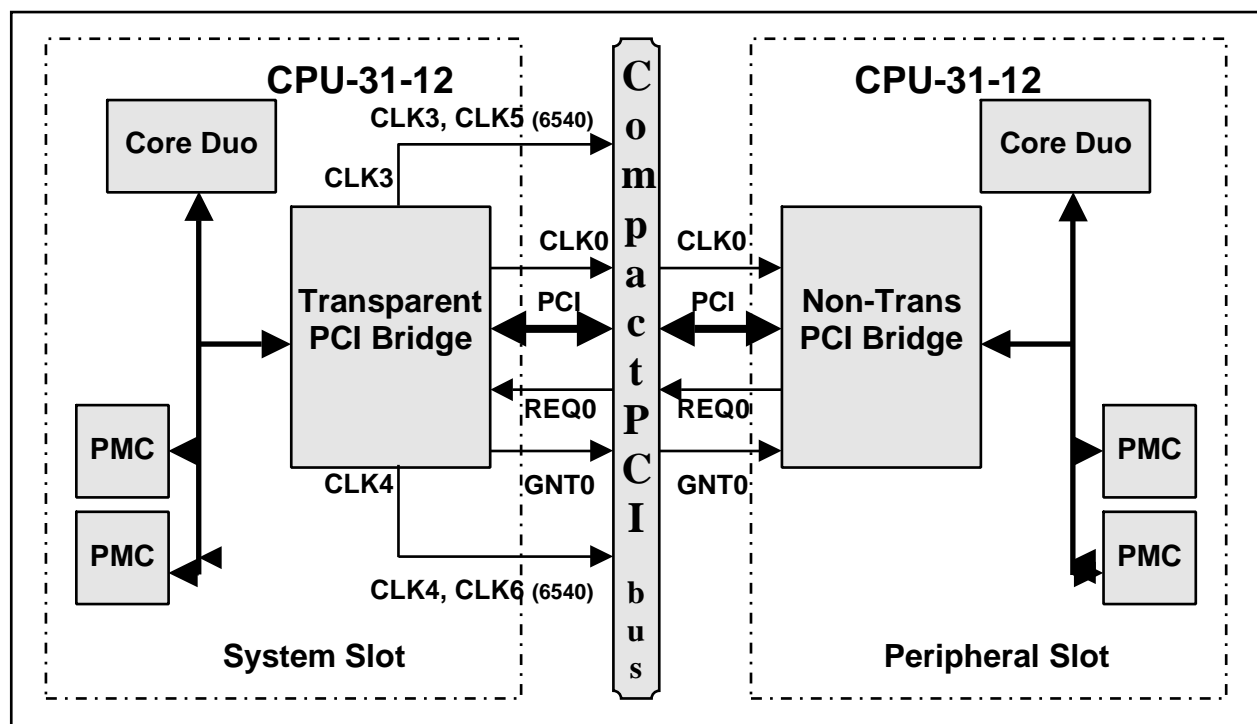
The PCI-X to cPCI-X interface, based on the PLX PCI 6540, offers the following features:

- 64-bit PCI-X r1.0b compliant asynchronous operation (limited to 66MHz by the 6300ESB south bridge)
- 10 KB FIFO for efficient PCI-X to PCI-X bridging and speed conversion.
- Transparent and non-transparent bridge operation.
- Usable in the cPCI system slot or a peripheral slot.

- The block diagram of the PCI-PCI interface is shown below:



The 6540 is a universal bridges, meaning their mode of operation is determined by the SYSEN# signal on the cPCI backplane. In this application, the CPU-31-12 can be used without jumpers for the system slot or peripheral slot in a CompactPCI system. The bridge senses the type of slot (system or peripheral) and configures itself as *Transparent* or *Non-Transparent* respectively. In the system slot, the CPU is expected to operate as a host, and the bridge operates in Transparent mode. In the peripheral slot, the CPU is part of an intelligent subsystem, and the bridge is configured in Non-Transparent mode. The figure below shows:



This drawing shows how the CPU-31-12 operates differently depending on whether it's in the system slot on the backplane (denoted by a triangle) or one of the remaining peripheral slots (denoted by circles silkscreened on the backplane). When in the system slot the six additional REQ/GNT pairs and six additional clocks are routed to the backplane in compliance with the PICMG CompactPCI spec (though boards using the PCI6540 route CLK3 to the pins assigned to CLK3 and CLK5 and CLK4 to CLK4 and CLK6 because the 6540 only has five CLK output lines available). These additional CLK and REQ/GNT lines are not used when the CPU-31-12 is installed in a peripheral slot. They are in a tristate mode.

A *transparent* PCI bridge is meant to provide electrical isolation to the system. It allows additional loads (and devices) to be attached to the bus, and can also be used to operate dissimilar PCI Bus data widths and speeds on the same system. *For example*, a transparent bridge can allow several 32-bit, 33 MHz PCI devices to attach to a 64-bit, 66 MHz PCI-X slot. A *non-transparent* PCI bridge offers address isolation in addition to electrical isolation. Devices on both sides of the bridge retain their own independent Memory space, and data from one side of the bridge is forwarded to the other side, using an address translation mechanism. A non-transparent bridge is used when there is more than one intelligent entity (*such as* multiple processors) in the system. It is a common mechanism used for creating intelligent I/O cards and multi-processor systems.

The bridge is CompactPCI Hot Swap Ready, and complies with PICMG 2.1 R2.0 with High Availability Programming Interface level 1 (PI = 1).

The CPU-31-12 reset circuitry is tied to the bridge, since the CPU-31-12 can generate the cPCI SYSRESET* signal as well as be reset by another cPCI board that asserts the SYSRESET* signal. The CPU-31-12 reset circuitry is discussed in detail in Section 3.12.

This section supplements the PCI-to-PCI Bus Bridge documentation (downloadable from PLX Technology's website at http://www.plxtech.com/products/fastlane_bridges/default.asp), which contains comprehensive descriptions of the operation and programming of the PCI 6254 and PCI6540 devices.

3.8 PCI-X Mezzanine Card (PMC-X) and XMC Expansion

The CPU-31-12 supports two PCI-X Mezzanine Card (PMC-X) sites on-board. Site #1 also supports x8 XMC cards. Site #1 routes I/O from J14 out through the J5 connector (please see Appendix A) or it can be accessed from the front panel. Site #2 routes I/O from J24 to the J3 backplane connector and/or to the front panel.

3.9 Intel's FW82802AC Firmware Hub Holds the System BIOS In Flash Memory

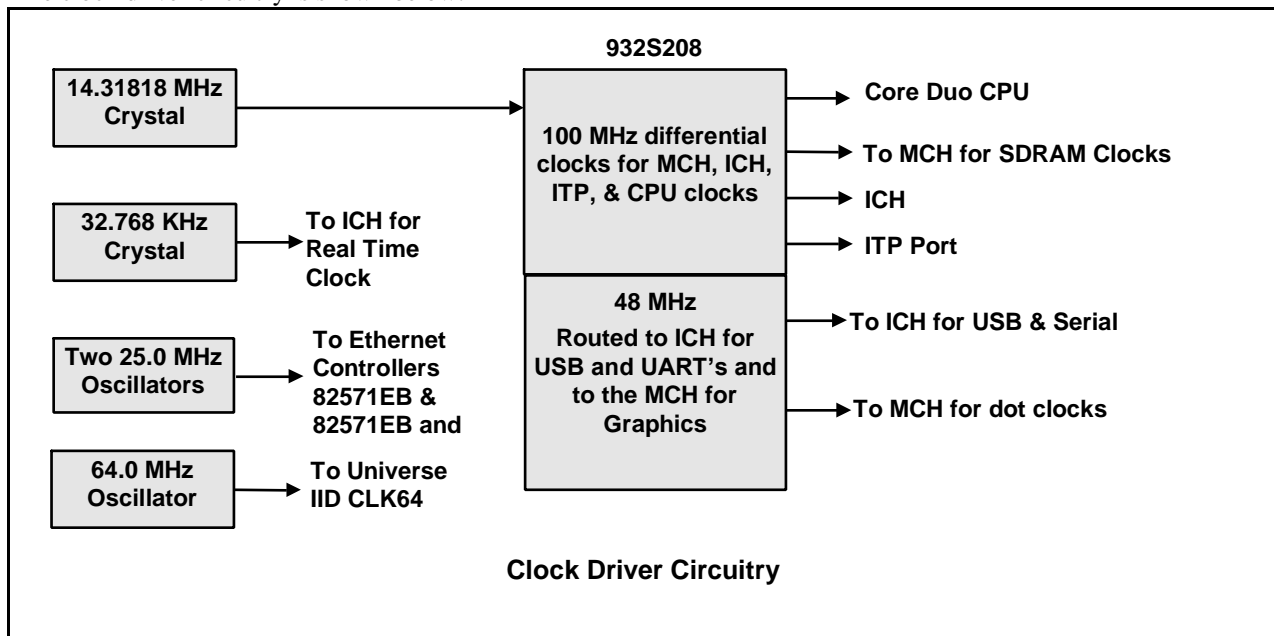
The Intel FW82802AC uses a 5-pin interface and provides 1 MByte of flash memory for the system BIOS. This device can fill the 1 MB real mode memory map so only a portion its upper 256 MB is used. The FW82802AC's 1 MB of memory space is segmented into sixteen parameter blocks of 64 KB each. The CPU-31-12 powers up into real mode and the BIOS is eventually shadowed into system DRAM after booting through the BIOS.

The ICH provides the 5-pin interface to the E82802AC. The upper 256 KB of the E82802AC is located from 000C0000 - 000FFFFF and its full 1 MB of memory is aliased from FFF00000 – FFFFFFFF where it can be fully accessed after booting up through the BIOS. Here's a link to a datasheet for the 82802AC:

<ftp://download.intel.com/design/chipsets/datashts/29065804.pdf>

3.10 Clock Drivers

The clock driver circuitry is shown below:



The clocks are generated by the 932S208, which is driven by a 14.31818 MHz crystal. DRAM clocks are synthesized by the MCH and Hub Interface and PCI(-X) clocks are produced by the ICH. A 32.768 KHz Crystal drives the Real Time Clock (RTC) on the ICH. The Fast Ethernet port provided to the front panel by the 82571EB and the two 1 Gb Ethernet ports provided to the backplane by the 82571EB require separate 25.0 MHz oscillators (one of the two oscillators is also used for the watchdog timer clock). A 64.0 MHz oscillator drives the Universe IID CA91C142D CompactPCI circuitry.

3.11 IPMI & Reset Circuitry & LEDs

The CPM1, with Pigeon Point System's Data Sentry system, implements the mandatory management interfaces defined by the PICMG 2.9 specification to be supported in connection with an IPM Controller.

Optional features are listed below. Several of these signals are required to be supported in cPCI boards that comply with specific PICMG 2.x specifications (such as PICMG 2.1 or PICMG 2.16 for the first four signals below), but with no corresponding requirement that the IPM Controller on a board have any particular responsibility or control regarding them.

- BD_SEL# signal
- Handle switch
- Hot swap LED
- HEALTHY# signal
- Fan control and monitoring

There are multiple ways to perform a hard reset of the CPM1:

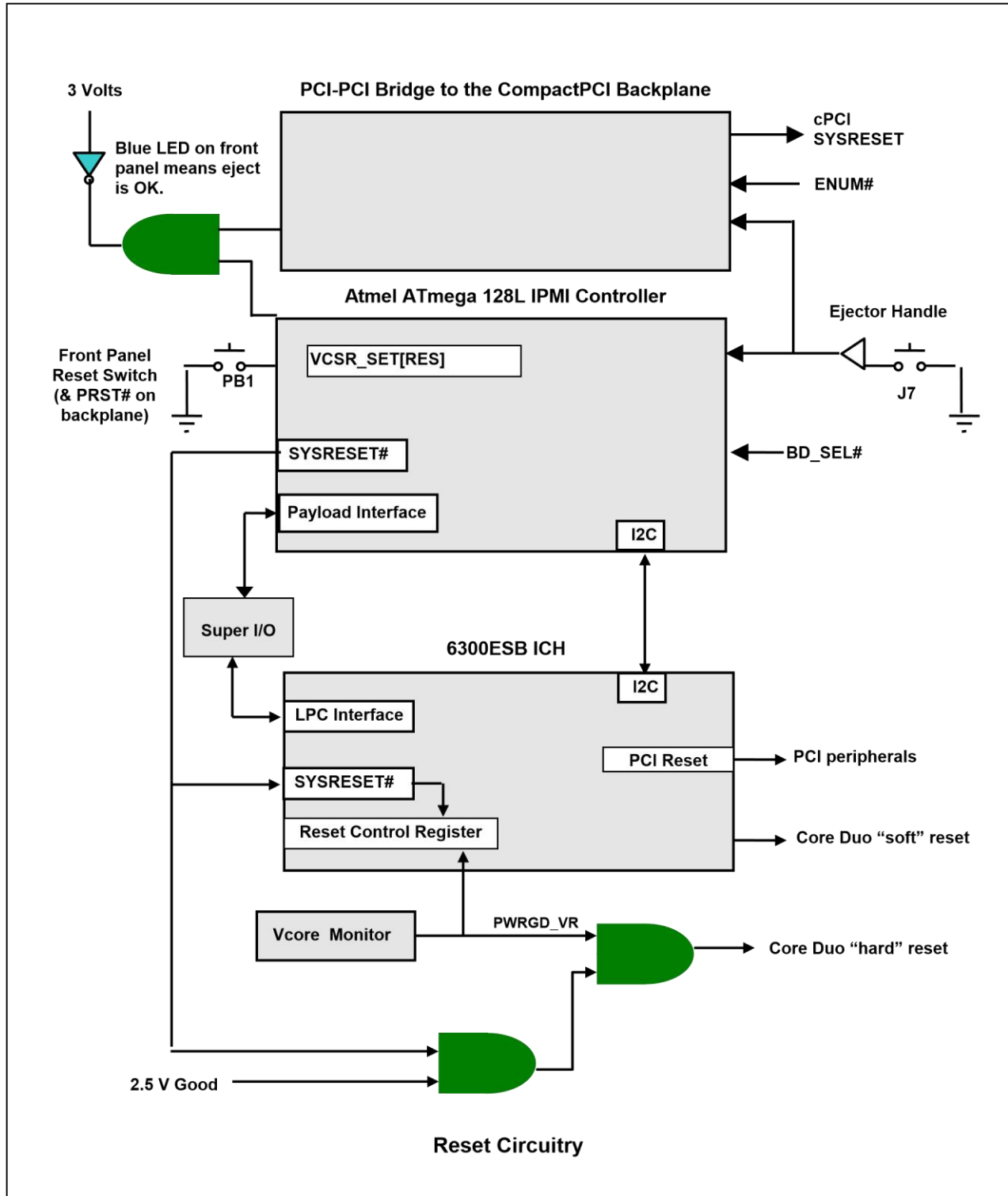
- A simple power cycle (turn the chassis' power off and on).
- There are two options for using a push button reset: the momentary push button switch that's accessible at the CPM1's front panel near the lower ejector handle; the PRST# signal on the backplane (connector J2, pin C17) that is generally connected to the chassis' reset button.
- When the CPM1 is installed in a peripheral slot it can be reset by the system controller module through a conventional PCI Reset.
- A DS1233 monitors the on-board 3.3 VDC, regulated from the 5.0 VDC off the backplane, and provides proper power sequencing for the CPU.
- A hot swap removal of the CPM1 from the chassis. When the ejector handles are released and the blue front panel LED is lit, the board has been reset and it is safe to remove the CPM1 completely from the chassis

For further information on the peripherals that play a part in the reset circuitry, refer to ICH datasheet that's referenced in Section 2.

There are four FRU LEDs that are routed from the IPMI controller and they are located near the front panel on the solder side of the CPM1 under PMC site #2. These LEDs cannot be seen when through the front panel. Here is the signal – LED correspondence:

Atmel ATmega 128L IPMI Controller Pin	LED
MOSI/PB2	D11 Green
MISO/PB3	D11 Red
OC0/PB4	D12 Green
OC1/PB5	D12 Red

The reset circuitry is shown below:



4. Installation

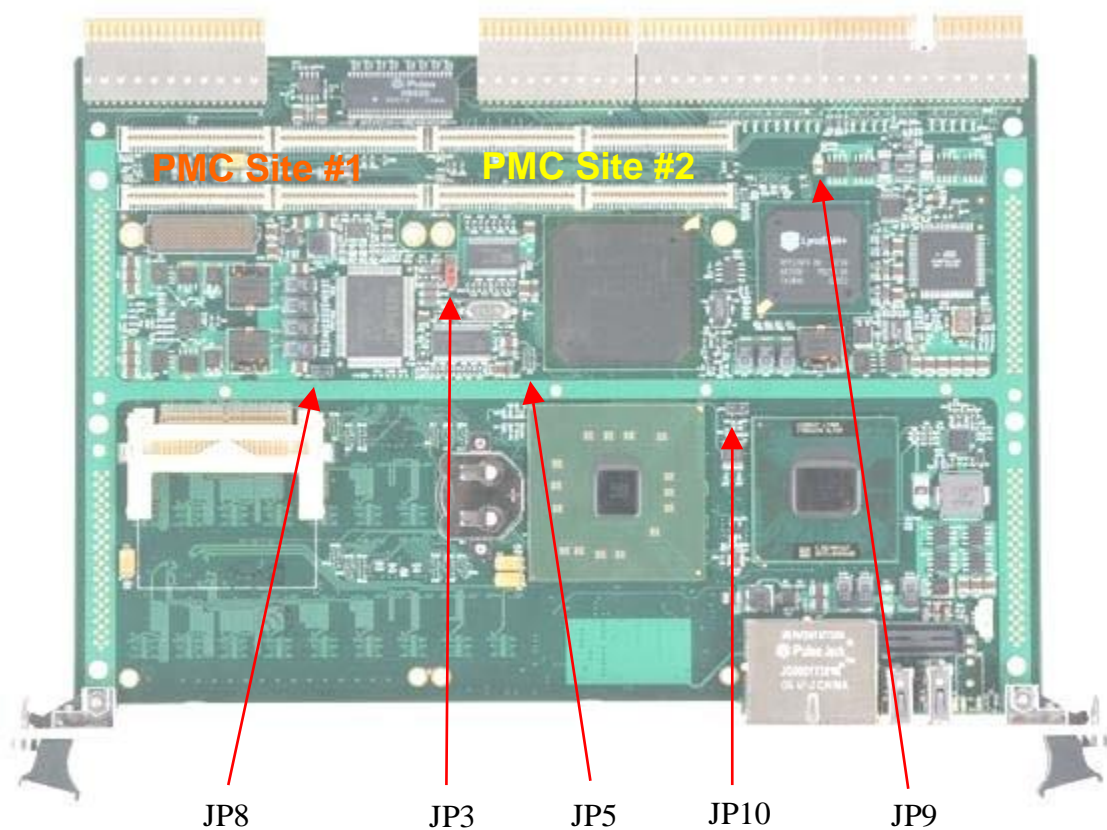
The following sections cover the steps necessary to configure the CPU-31-12 and install it into a CompactPCI system for single-slot operation. This chapter should be read in its entirety before proceeding with the installation.

4.1 Selectable Options

This section explains how to set up user configurable jumpers and how to install CompactFlash drives and PMC modules.

The CPU-31-12 is shipped in an antistatic bag. Be sure to observe proper handling procedures during the configuration and installation process, to avoid damage due to electrostatic discharge (ESD).

The CPU-31-12 contains 5 jumpers. JP9 does not have posts as it should not be shunted by the user.



Chapter 4 – Installation

The CPM1 offers a number of user configurable hardware options.

Jumpers	Description
JP3	Determines VIO for the PMC sites 1 & 2 (1 – 2 for 3.3 VDC; 2 – 3 for 5.0 VDC)
JP5	Close momentarily to flush RTC and NV-RAM and revert to BIOS defaults
JP8	MUST STAY OPEN (on-board BIOS is disabled when closed)
JP9	Grounds PRV_DEV/XB_MEM when shunted
JP10	Grounds GPIO43 when closed, used to reset BIOS settings in systems w/o battery backup

Jumper JP3 selects the VIO routed to the CPM1's PMC modules. The VIO pins determine the signaling voltage on the PMC(X) modules' PCI(-X) interface. Refer to the PMC module's reference manual to ascertain the recommended VIO. Shunting pins 1 & 2 of JP2 & JP3 provides a VIO of 3.3 VDC. Shunting between pins 2 & 3 routes 5 VDC to the VIO pins on the PMC(X) module.

VIO Voltage Level	JP3
3.3 VDC (Necessary for PCI-X Operation)	1-2
5 VDC	2-3

PMC Signaling Voltage Selection

Switch JP5 should be closed momentarily (for about 30 seconds) to restore the default BIOS settings. SW1-8 should always be closed (in the "on" position) – this switch is used for factory use.

Jumper JP9 determines the status of PRV_DEV/XB_MEM.

PRV_DEV(when in the Transparent Mode):

When set to 1, the PCI 6540 can mask secondary devices using IDSEL connected to S_AD[23:16] as private devices. Any Type 1 Configuration access to these IDSELs is routed to AD24. If there is no device on S_AD24, the re-routed Type 1 Configuration cycles are Master Aborted. The PCI 6540 also reserves Private Memory space for the secondary port. The Memory space can be programmed using the Private Memory Base and Limit registers (Base—PVTMBAR; PCI:6Ch and VTMBARU32; PCI:70h, Limit—VTMLMT; PCI:6Eh and PVTMLMTU32; PCI:74h). If the limit is smaller than the base, Private Memory space is disabled. The primary port cannot access this Memory space through the bridge and the secondary port does not respond to Memory cycles addressing this Private Memory space.

XB_MEM(when in the Non-Transparent Mode):

When set to 1, the PCI 6540 automatically claims 16 MB of Memory space. This allows the boot-up of the LowPriority Boot port to proceed without waiting for the Priority Boot port to program the corresponding Memory Base Address registers (BARs). Although the default claims 16 MB, the BARs can be modified by serial EEPROM or software to change the window size. If XB_MEM=1, the P_PORT_READY or S_PORT_READY mechanism is not relevant. Also, if XB_MEM=1, the PCI 6540 autoloads serial EEPROM data up to Group 5 instead of Group 4.

PRV_DEV/XB_MEM	JP9
Grounded, Logic 0	Closed
Logic 1	Open

Chapter 4 – Installation

4.2 CompactFlash Drive Installation

The CPU-31-12 supports a bootable CompactFlash Drive for booting up into an Operating System (OS) while occupying only one slot in the CompactPCI chassis. Connector J3 is a Type II CompactFlash connector and is used for this purpose. J3 is located below PMC site 1.

4.3 PCI Mezzanine Card (PMC) Installation

The CPU-31-12 supports two PMC add-on module sites that let the user expand the CPU-31-12's local I/O with PCI Mezzanine Cards (PMC) or PMCX (PMC modules capable of PCI-X transfers) modules. The PMCX sites are backwards compatible and can support any modules from 32-bit PMC cards at 33 MHz to 64-bit PMCX modules at 66 MHz.

The PMCX sites on the CPU-31-12 are routed from the ICH's PCI-X bus interface which is 64 bits wide and has a maximum clock rate of 66 MHz.

PMCX sites	Available Data Rates with VIO = 5 V (JP3 is shunted between pins 2 & 3)	Available Data Rates with VIO = 3.3 V (JP3 is shunted between pins 1 & 2)
1 & 2	33 MHz	33 MHz and 66 MHz

The General Software BIOS will determine during startup what the status of the PCI-X bus. The BIOS monitors the following pins that are routed to the ICH: PCIXCAP (PCX-X capable) and M66EN (66 MHz capable). The user's manual on your PMC(X) modules will tell you how PCIXCAP (JN1, pin 39) and M66EN (JN2, pin 47) are configured. Since both sites share the same bus, JP3 sets the VIO voltage for both sites and the bus will only clock as fast as the slower PMC card.

Conventionally PMC connectors have four designators: JN1 – JN4. JN1 & JN2 provide all the signals necessary for 32-bit PCI transactions, JN3 has the 32 additional data lines required for 64-bit transfers, and JN4 routes I/O off the module for possible backplane access (see Section A for J14 to J5 and J24 to J3 backplane PMCX I/O routing). The following table lists the reference designators used on the CPU-31-12's PMC(X) sites:

PMCX site	JN1	JN2	JN3	JN4
1 (also supports XMC)	J11	J12	J13	J14 (to J5)
2	J21	J22	J23	J24 (to J3)

4.5 Front Panel Connectors and Reset Switch

The CPU-31-12 offers front panel connections for two USB ports and two RJ45 connector for 1000BaseTX Ethernet ports. Install all front panel cables by inserting them into the appropriate connector. COM1 and DVO/VGA cables can be secured to the CPU-31-12 by tightening their thumbscrews into the connectors' jackscrews. USB and Ethernet mating connectors should snap into place. Mounting hardware for the front panel connectors are isolated from the CPU-31-12's digital ground. They are continuous with the front panel itself that, in turn, is common with chassis ground.

The CPU-31-12 contains a recessed reset switch, accessible from the front panel. To reset the CPU-31-12, press the reset switch using a small screwdriver blade or similar implement.

The Ethernet connectors each have a pair of indicator LEDs built in. These two green LEDs offer stats on the 1000BaseTX port provided by the 82571EB Ethernet controller on the CPU-31-12.

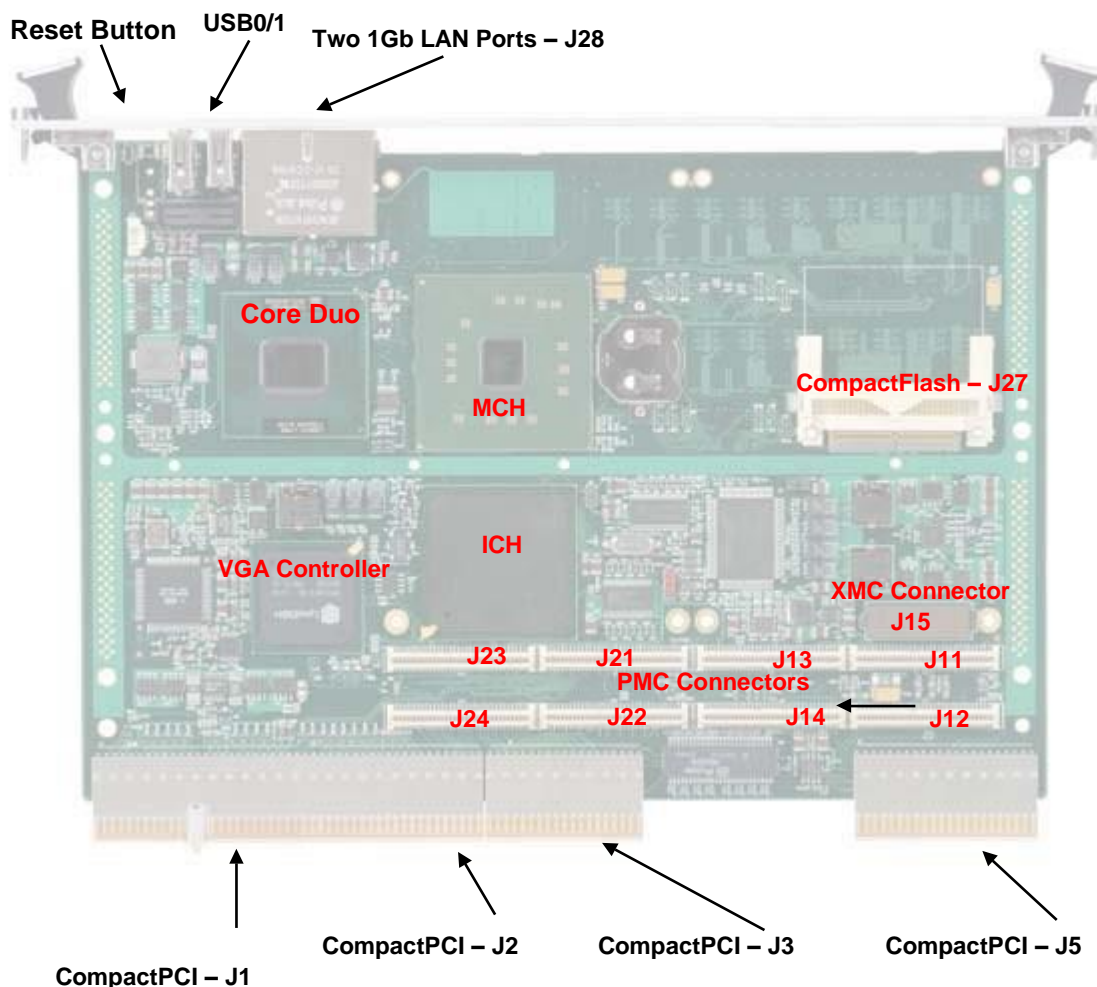
□□ **Link** – Ethernet link is established when on. This LED is to the left (or top when the CPU-31-12 is held vertically)

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□□ **Activity** – Ethernet data is being transmitted from or received by the CPU-31-12 when on. This LED is to the right/bottom of the Link LED.

A. Connector Pin-outs

The locations of the CPU-31-12 connectors are shown below. The connectors that do not go to the front panel have their pin 1 location designated accordingly.



A.1 Front Panel USB Connector (USB1 & USB2)

There are two USB connectors (labeled USB1 & USB2) accessible at the CPU-31-12's front panel. Though they are separate ports, their pin-outs are identical so the following table offers the pin-out of one connector as both.

Pin	Signal Description
1	+5 VDC (via 1.1 amp self-resetting fuse F2)
2	Negative Data
3	Positive Data
4	Signal GND
5	Chassis GND
6	Chassis GND
7	Chassis GND
8	Chassis GND

Appendix A – Connector Pin-outs

USB Connectors (USB1 & USB2) – Front Panel USB Receptacles. The metal shell of the connector goes to chassis ground.

A.2 1000BaseTX Fast Ethernet Front Panel Connector (J28)

The CPU-31-12 uses a dual RJ45 connector to provide two 1000BaseTX Ethernet ports at the front panel. Though there are two separate ports in one connector, the pin-outs are identical so the following table offers the pin-out of one connector as both.

Pin	Signal Description	Signal Description
1	Negative Data 0	MX0-
2	Positive Data 0	MX0+
3	Negative Data 1	MX1-
4	Positive Data 1	MX1+
5	Negative Data 2	MX2-
6	Positive Data 2	MX2+
7	Negative Data 3	MX3-
8	Positive Data 3	MX3+

1000BaseTX Fast Ethernet Connector (J28) – Front Panel RJ-45 Connector. The metal shell of the connector goes to chassis ground.

A.3 CompactFlash Interface Connector (J27)

Pin	Signal	Pin	Signal
1	GND	26	No connection
2	D3	27	D11
3	D4	28	D12
4	D5	29	D13
5	D6	30	D14
6	D7	31	D15
7	CS1#	32	CS3#
8	GND	33	No connection
9	GND	34	DIOR#
10	GND	35	DIOW#
11	GND	36	+5 VDC
12	GND	37	DIRQ (IRQ15)
13	+5 VDC	38	+5 VDC
14	GND	39	Pulled Low (master)
15	GND	40	No connection
16	GND	41	IDERESET
17	GND	42	Pulled Up to 3.3 VDC

18	DA2	43	DMA REQ
19	DA1	44	DMA ACK#
20	DA0	45	No connection
21	D0	46	Pull-up to +5 VDC
22	D1	47	D8
23	D2	48	D9
24	No connection	49	D10
25	No connection	50	GND

CompactFlash Type II Interface Connector (J27)

A.4 cPCI Connectors (J1, J2, J3, and J5)

Connectors J1 and J2 bring a 64-bit 66 MHz capable PCI-X bus to the CompactPCI backplane. “PU” stands for “pulled up”.

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A25	5 VDC	B25	REQ64#	C25	ENUM#	D25	3.3 VDC	E25	5 VDC
A24	AD1	B24	5 VDC	C24	VI/OL	D24	AD0	E24	ACK64#
A23	3.3 VDC	B23	AD4	C23	AD3	D23	5 VDC L	E23	AD2
A22	AD7	B22	GND	C22	3.3 VDC L	D22	AD6	E22	AD5
A21	3.3 VDC	B21	AD9	C21	AD8	D21	M66EN	E21	C/BE0#
A20	AD12	B20	GND	C20	VI/O	D20	AD11	E20	AD10
A19	3.3 VDC	B19	AD15	C19	AD14	D19	GND	E19	AD13
A18	SERR#	B18	GND	C18	3.3 VDC	D18	PAR	E18	C/BE1#
A17	3.3 VDC	B17	IPMB SCL	C17	IPMB SDA	D17	GND	E17	PERR#
A16	DEVSEL#	B16	PCIXCAP	C16	VI/O	D16	STOP#	E16	LOCK#
A15	3.3 VDC	B15	FRAME#	C15	IRDY#	D15	BDSEL#	E15	TRDY#
A14	KEY1: NC	B14	KEY4: NC	C14	KEY7: NC	D14	KEY10: NC	E14	KEY13: NC
A13	KEY2: NC	B13	KEY5: NC	C13	KEY8: NC	D13	KEY11: NC	E13	KEY14: NC
A12	KEY3: NC	B12	KEY6: NC	C12	KEY9: NC	D12	KEY12: NC	E12	KEY15: NC
A11	AD18	B11	AD17	C11	AD16	D11	GND	E11	C/BE2#
A10	AD21	B10	GND	C10	3.3 VDC	D10	AD20	E10	AD19
A09	C/BE3#	B09	IDSEL	C09	AD23	D09	GND	E09	AD22
A08	AD26	B08	GND	C08	VI/O	D08	AD25	E08	AD24
A07	AD30	B07	AD29	C07	AD28	D07	GND	E07	AD27
A06	REQ0#	B06	PCI_PRESENT#	C06	3.3 VDC L	D06	CLK0	E06	AD31
A05	RESVD: NC	B05	RESVD: NC	C05	RST#	D05	GND	E05	GNT0#
A04	IPMB PWR: NC	B04	HEALTHY#	C04	VI/OL	D04	INTP	E04	INTS
A03	INTA#	B03	INTB#	C03	INTC#	D03	5 VDC L	E03	INTD#
A02	TCK: NC	B02	5 VDC	C02	TMS: NC	D02	TDO: NC	E02	TDI: NC

Appendix A – Connector Pin-outs

A01	5 VDC	B01	-12 VDC: NC	C01	TRST#: NC	D01	+12 VDC	E01	5 VDC
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CompactPCI Backplane Connector (J1) – Row F is grounded

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A22	GA4	B22	GA3	C22	GA2	D22	GA1	E22	GA0
A21	CLK6	B21	GND	C21	RESVD: NC	D21	RESVD: NC	E21	RESVD: NC
A20	CLK5	B20	GND	C20	RESVD: NC	D20	GND	E20	RESVD: NC
A19	GND	B19	GND	C19	RESVD: NC	D19	RESVD: NC	E19	RESVD: NC
A18	RESVD: NC	B18	RESVD: NC	C18	RESVD: NC	D18	GND	E18	RESVD: NC
A17	RESVD: NC	B17	GND	C17	PRST#	D17	REQ6#	E17	GNT6#
A16	RESVD: NC	B16	RESVD: NC	C16	DEG# (Pulled Up)	D16	GND	E16	RESVD: NC
A15	RESVD: NC	B15	GND	C15	FAL# (Pulled Up)	D15	REQ5#	E15	GNT5#
A14	AD35	B14	AD34	C14	AD33	D14	GND	E14	AD32
A13	AD38	B13	GND	C13	VI/O	D13	AD37	E13	AD36
A12	AD42	B12	AD41	C12	AD40	D12	GND	E12	AD39
A11	AD45	B11	GND	C11	VI/O	D11	AD44	E11	AD43
A10	AD49	B10	AD48	C10	AD47	D10	GND	E10	AD46
A09	AD52	B09	GND	C09	VI/O	D09	AD51	E09	AD50
A08	AD56	B08	AD55	C08	AD54	D08	GND	E08	AD53
A07	AD59	B07	GND	C07	VI/O	D07	AD58	E07	AD57
A06	AD63	B06	AD62	C06	AD61	D06	GND	E06	AD60
A05	C/BE5#	B05	64EN#	C05	VI/O	D05	C/BE4#	E05	PAR64
A04	VI/O	B04	RESVD: NC	C04	C/BE7#	D04	GND	E04	C/BE6#
A03	CLK4	B03	GND	C03	GNT3#	D03	REQ4#	E03	GNT4#
A02	CLK2	B02	CLK3	C02	SYSEN#	D02	GNT2#	E02	REQ3#
A01	CLK1	B01	GND	C01	REQ1#	D01	GNT1#	E01	REQ2#

CompactPCI Backplane Connector (J2) – Row F is grounded

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A19	RESVD: NC	B19	RESVD: NC	C19	RESVD: NC	D19	RESVD: NC	E19	RESVD: NC
A18	LPa_DA+	B18	LPa_DA-	C18	GND	D18	LPa_DC+	E18	LPa_DC-
A17	LPa_DB+	B17	LPa_DB-	C17	GND	D17	LPa_DD+	E17	LPa_DD-
A16	LPb_DA+	B16	LPb_DA-	C16	GND	D16	LPb_DC+	E16	LPb_DC-
A15	LPb_DB+	B15	LPb_DB-	C15	GND	D15	LPb_DD+	E15	LPb_DD-
A14	3.3 VDC	B14	3.3 VDC	C14	3.3 VDC	D14	5 VDC	E14	5 VDC
A13	PMCI/O pin 5	B13	PMCI/O pin 4	C13	PMCI/O pin 3	D13	PMCI/O pin 2	E13	PMCI/O pin 1
A12	PMCI/O pin 10	B12	PMCI/O pin 9	C12	PMCI/O pin 8	D12	PMCI/O pin 7	E12	PMCI/O pin 6
A11	PMCI/O pin 15	B11	PMCI/O pin 14	C11	PMCI/O pin 13	D11	PMCI/O pin 12	E11	PMCI/O pin 11
A10	PMCI/O pin 20	B10	PMCI/O pin 19	C10	PMCI/O pin 18	D10	PMCI/O pin 17	E10	PMCI/O pin 16
A09	PMCI/O pin 25	B09	PMCI/O pin 24	C09	PMCI/O pin 23	D09	PMCI/O pin 22	E09	PMCI/O pin 21
A08	PMCI/O pin 30	B08	PMCI/O pin 29	C08	PMCI/O pin 28	D08	PMCI/O pin 27	E08	PMCI/O pin 26

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A07	PMCI/O pin 35	B07	PMCI/O pin 34	C07	PMCI/O pin 33	D07	PMCI/O pin 32	E07	PMCI/O pin 31
A06	PMCI/O pin 40	B06	PMCI/O pin 39	C06	PMCI/O pin 38	D06	PMCI/O pin 37	E06	PMCI/O pin 36
A05	PMCI/O pin 45	B05	PMCI/O pin 44	C05	PMCI/O pin 43	D05	PMCI/O pin 42	E05	PMCI/O pin 41
A04	PMCI/O pin 50	B04	PMCI/O pin 49	C04	PMCI/O pin 48	D04	PMCI/O pin 47	E04	PMCI/O pin 46
A03	PMCI/O pin 55	B03	PMCI/O pin 54	C03	PMCI/O pin 53	D03	PMCI/O pin 52	E03	PMCI/O pin 51
A02	PMCI/O pin 60	B02	PMCI/O pin 59	C02	PMCI/O pin 58	D02	PMCI/O pin 57	E02	PMCI/O pin 56
A01	VIO_PX	B01	PMCI/O pin 64	C01	PMCI/O pin 63	D01	PMCI/O pin 62	E01	PMCI/O pin 61

CompactPCI Backplane Connector (J3) – Row F is grounded

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A22	XIO5	B22	XIO4	C22	XIO3	D22	XIO2	E22	XIO1
A21	XIO10	B21	XIO9	C21	XIO8	D21	XIO7	E21	XIO6
A20	XIO15	B20	XIO14	C20	XIO13	D20	XIO12	E20	XIO11
A19	XIO20	B19	XIO19	C19	XIO18	D19	XIO17	E19	XIO16
A18	XIO25	B18	XIO24	C18	XIO23	D18	XIO22	E18	XIO21
A17	XIO30	B17	XIO29	C17	XIO28	D17	XIO27	E17	XIO26
A16	XIO35	B16	XIO34	C16	XIO33	D16	XIO32	E16	XIO31
A15	XIO40	B15	XIO39	C15	XIO38	D15	XIO37	E15	XIO36
A14	XIO45	B14	XIO44	C14	XIO43	D14	XIO42	E14	XIO41
A13	XIO50/PD1	B13	XIO49/PD0	C13	XIO48	D13	XIO47	E13	XIO46
A12	XIO55/PD6	B12	XIO54/PD5	C12	XIO53/PD4	D12	XIO52/PD3	E12	XIO51/PD2
A11	XIO60/GP13	B11	XIO59/GP12	C11	XIO58/GP11	D11	XIO57/GP10	E11	XIO56/PD7
A10	COM2 RI#/RxD-	B10	XIO64/GP17	C10	XIO63/GP16	D10	XIO62/GP15	E10	XIO61/GP14
A09	COM2 DTR/RxD+	B09	COM1 DTR	C09	VGA RED	D09	LINKA	E09	Keybrd Data
A08	COM2 CTS/CTS-	B08	COM1 CTS	C08	VGA GREEN	D08	ACT A	E08	Keyboard Clk
A07	COM2 TxD#/CTS+	B07	COM1 TxD#	C07	VGA BLUE	D07	LINKB	E07	Mouse Data
A06	COM2 RTS/RTS+	B06	COM1 RTS	C06	VGA HSYNC	D06	ACT B	E06	Mouse Clock
A05	COM2 RxD#/RTS-	B05	COM1 RxD#	C05	VGA VSYNC	D05	SPKR	E05	USB 5VDC
A04	COM2 DSR/TxD+	B04	COM1 DSR	C04	VGA ddcdata	D04	No Connect	E04	USB_P2N
A03	COM2 DCD/TxD-	B03	COM1 DCD	C03	VGA ddcclk	D03	SATA_LED#	E03	USB_P2P
A02	SATA1_RXP	B02	SATA1_RXN	C02	SATA1_TXN	D02	SATA1_TXP	E02	USB_P3N
A01	SATA0_RXP	B01	SATA0_RXN	C01	SATA0_TXN	D01	SATA0_TXP	E01	USB_P3P

CompactPCI Backplane Connector (J5) With Custom I/O Option Resistors – Row F is grounded

COM2 can be custom configured as an RS4xx port at the factory. These signals are shown in the table above in **red font**. GPIO lines from the Super I/O chip are shown in **green font**. CPU-31-12s with these options need special ordering.

The following table shows which signals are routed to the backplane (instead of PMC Site #1 I/O pins from J14 labeled as XIOx in the table above) when their associated zero ohm resistors are populated. The R# columns provide the resistor numbers as shown on the CPU-31-12's printed circuit board's silkscreen. For example, adding

Appendix A – Connector Pin-outs

resistor R770 will route COM4's DSR signal to pin D16 on J5. These optional 0 ohm resistors can route the Ring lines for COM1 & COM2 (with R736 and R737 respectively), COM3, COM4, and the IDE bus to J5. The IDE bus signals are printed in [blue font](#).

Pin	R#	Row A	R#	Row B	R#	Row C	R#	Row D	R#	Row E
22	685	PDD8	684	PDD7	683	IRQ14	695	COM4 RI	689	COM3 RI
21	688	PDD9	687	PDD6	686	PRI RST#	700	COM4 DTR	694	COM3 DTR
20	693	PDD10	692	PDD5	696	PDDREQ	705	COM4 CTS	699	COM3 CTS
19	698	PDD11	697	PDD4	701	PDIOW#	710	COM4 Tx#	704	COM3 Tx#
18	703	PDD12	702	PDD3	706	PDIOR#	715	COM4 RTS	709	COM3 RTS
17	708	PDD13	707	PDD2	711	PIORDY	731	COM4 Rx#	714	COM3 Rx#
16	713	PDD14	712	PDD1	716	PDDACK#	770	COM4 DSR	727	COM3 DSR
15	718	PDD15	717	PDD0	726	PDA2	773	COM4 DCD	772	COM3 DCD
14	-	-	721	PDA1	730	PDCS1#	-	-	-	-
13	-	-	725	PDA0	729	PDCS3#	-	-	-	-
10	737	COM2 RI	736	COM1 RI	-	-	-	-	-	-

CompactPCI Backplane Connector (J5) With I/O Option Resistors – Row F is grounded

A.5 PCI-X Mezzanine Card Connectors (JN1, JN2, JN3, and JN4) and the XMC connector (J15)

This section has the pin-outs for all four PMC connectors. There are two PMC sites. Their pinouts are largely identical. When signals differ between the two PMC sites, **red font will be used for PMC Site 1 (connectors J11 – J14)** (see the photo at the beginning of Section 4 of this User's Manual) and **blue font will be used for PMC Site 2 (connectors J21 – J24)**. JN4 pinouts for the two different sites, I/O connectors where the pins are routed to J5 & J3 respectively, are completely different for the two sites so these pinouts will be provided separately.

Pin	Signal	Pin	Signal
1	5.6K pull-down	2	-12 VDC
3	GND	4	INTF#/PX_PIRQ1#
5	INTG#/PX_PIRQ2#	6	INTH#/PX_PIRQ3#
7	No connection	8	+5 VDC
9	INTE#/PX_PIRQ0#	10	No connection
11	GND	12	No connection
13	PMC1CLK/PMC1CLK	14	GND
15	GND	16	GNT0#/GNT1#
17	REQ0#/REQ1#	18	+5 VDC
19	VI/O from JP3	20	AD31
21	AD28	22	AD27
23	AD25	24	GND
25	GND	26	C/BE3#
27	AD22	28	AD21
29	AD19	30	+5 VDC
31	VI/O from JP3	32	AD17
33	FRAME#	34	GND
35	GND	36	IRDY#
37	DEVSEL#	38	+5 VDC
39	PCIXCAP	40	LOCK#
41	No connection	42	No connection
43	PAR	44	GND
45	VI/O from JP3	46	AD15
47	AD12	48	AD11
49	AD9	50	+5 VDC
51	GND	52	C/BE0#
53	AD6	54	AD5
55	AD4	56	GND
57	VI/O from JP3	58	AD3
59	AD2	60	AD1
61	AD0	62	+5 VDC

Appendix A – Connector Pin-outs

63	GND	64	REQ64#
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PCI-X Mezzanine Card (PMC-X) Connector (JN1) – Molex 71439-0164

VIO is jumper selectable through JP3 (please see Section 4.1).

Pin	Signal	Pin	Signal
1	+12 VDC	2	TRST (pulled down)
3	TMS (pulled up)	4	No connection
5	TDI (pulled up)	6	GND
7	GND	8	No connection
9	No connection	10	No connection
11	+3.3 VDC	12	+3.3 VDC
13	PCI RST#	14	GND
15	+3.3 VDC	16	GND
17	No connection	18	GND
19	AD30	20	AD29
21	GND	22	AD26
23	AD24	24	+3.3 VDC
25	(IDSEL) AD17 / AD18	26	AD23
27	+3.3 VDC	28	AD20
29	AD18	30	GND
31	AD16	32	C/BE2#
33	GND	34	No connection
35	TRDY#	36	+3.3 VDC
37	GND	38	STOP#
39	PERR#	40	GND
41	+3.3 VDC	42	SERR#
43	C/BE1#	44	GND
45	AD14	46	AD13
47	M66EN	48	AD10
49	AD8	50	+3.3 VDC
51	AD7	52	No connection
53	+3.3 VDC	54	No connection
55	No connection	56	GND
57	No connection	58	No connection
59	GND	60	No connection
61	ACK64#	62	+3.3 VDC

63	GND	64	No connection
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PCI-X Mezzanine Card (PMCX) Connector (JN2) – Molex 71439-0164

Pin	Signal	Pin	Signal
1	No connection	2	GND
3	GND	4	C/BE7#
5	C/BE6#	6	C/BE5#
7	C/BE4#	8	GND
9	VIO	10	PAR64
11	AD63	12	AD62
13	AD61	14	GND
15	GND	16	AD60
17	AD59	18	AD58
19	AD57	20	GND
21	VIO	22	AD56
23	AD55	24	AD54
25	AD53	26	GND
27	GND	28	AD52
29	AD51	30	AD50
31	AD49	32	GND
33	GND	34	AD48
35	AD47	36	AD46
37	AD45	38	GND
39	VIO	40	AD44
41	AD43	42	AD42
43	AD41	44	GND
45	GND	46	AD40
47	AD39	48	AD38
49	AD37	50	GND
51	GND	52	AD36
53	AD35	54	AD34
55	AD33	56	GND
57	VIO	58	AD32
59	No connection	60	No connection
61	No connection	62	GND
63	GND	64	No connection

PCI-X Mezzanine Card (PMCX) Connector (JN3) – Molex 71439-0164

Pin	Signal	Pin	Signal
1	E22	2	D22
3	C22	4	B22
5	A22	6	E21
7	D21	8	C21
9	B21	10	A21
11	E20	12	D20
13	C20	14	B20
15	A20	16	E19
17	D19	18	C19
19	B19	20	A19
21	E18	22	D18
23	C18	24	B18
25	A18	26	E17
27	D17	28	C17
29	B17	30	A17
31	E16	32	D16
33	C16	34	B16
35	A16	36	E15
37	D15	38	C15
39	B15	40	A15
41	E14	42	D14
43	C14	44	B14
45	A14	46	E13
47	D13	48	C13
49	B13	50	A13
51	E12	52	D12
53	C12	54	B12
55	A12	56	E11
57	D11	58	C11
59	B11	60	A11
61	E10	62	D10
63	C10	64	B10

PCI-X Mezzanine Card (PMCX) Site #1 Connector (J14) – Molex 71439-0164

J14 is the JN4 I/O connector for PMC Site #1. These lines will be routed to the J5 backplane connector. The pins are given above.

Pin	Signal	Pin	Signal
1	E13	2	D13
3	C13	4	B13
5	A13	6	E12
7	D12	8	C12
9	B12	10	A12
11	E11	12	D11
13	C11	14	B11
15	A11	16	E10
17	D10	18	C10
19	B10	20	A10
21	E9	22	D9
23	C9	24	B9
25	A9	26	E8
27	D8	28	C8
29	B8	30	A8
31	E7	32	D7
33	C7	34	B7
35	A7	36	E6
37	D6	38	C6
39	B6	40	A6
41	E5	42	D5
43	C5	44	B5
45	A5	46	E4
47	D4	48	C4
49	B4	50	A4
51	E3	52	D3
53	C3	54	B3
55	A3	56	E2
57	D2	58	C2
59	B2	60	A2
61	E1	62	D1
63	C1	64	B1

Appendix A – Connector Pin-outs

PCI-X Mezzanine Card (PMCX) Site #2 Connector (J24) – Molex 71439-0164

J24 is the JN4 I/O connector for PMC Site #2. These lines will be routed to the pins shown for the J3 backplane connector.

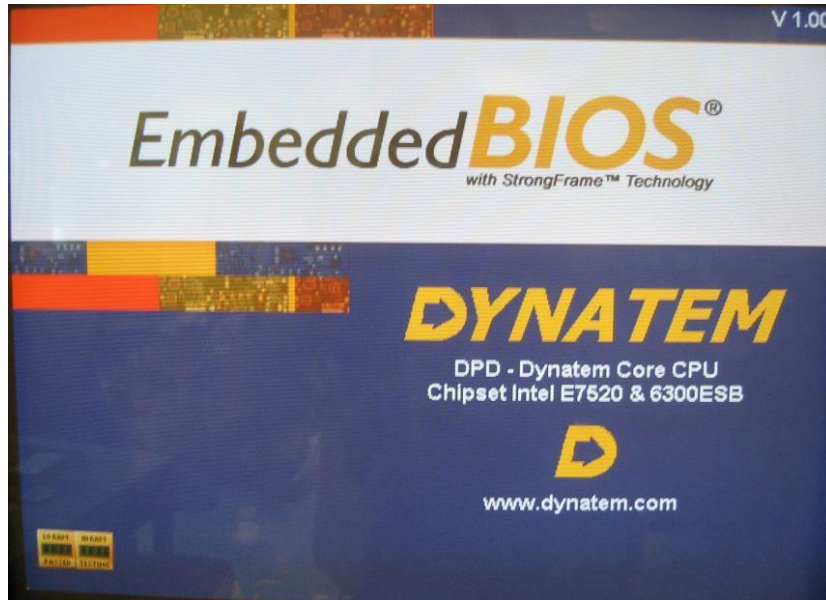
Following is the pinout for the XMC connector associated with PMC/XMC Site #1. The XMC site routes x8 PCI Express to the mezzanine card.

Pin	Column A	Column B	Column C	Column D	Column E	Column F
1	PETp08	PETn0B	3.3 VDC	PETp1B	PETn1B	5 VDC
2	Ground	Ground	TRST# pulled low	Ground	Ground	PCI_RST#
3	PETp2B	PETn2B	3.3 VDC	PETp3B	PETn3B	5 VDC
4	Ground	Ground	TCK pulled low	Ground	Ground	No Connect
5	PETp4B	PETn4B	3.3 VDC	PETp5B	PETn5B	5 VDC
6	Ground	Ground	TMS pulled high	Ground	Ground	12 VDC
7	PETp6B	PETn6B	3.3 VDC	PETp7B	PETn7B	5 VDC
8	Ground	Ground	TDI pulled high	Ground	Ground	-12 VDC
9	No Connect	No Connect	No Connect	No Connect	No Connect	5 VDC
10	Ground	Ground	No Connect	Ground	Ground	Ground
11	PERp0B	PERn0B	No Connect	PERp1B	PERn1B	5 VDC
12	Ground	Ground	Ground	Ground	Ground	No Connect
13	PERp2B	PERn2B	3.3 VDC	PERp3B	PERn3B	5 VDC
14	Ground	Ground	Ground	Ground	Ground	No Connect
15	PERp4B	PERn4B	No Connect	PERp5B	PERn5B	5 VDC
16	Ground	Ground	No Connect	Ground	Ground	No Connect
17	PERp6B	PERn6B	No Connect	PERp7B	PERn7B	No Connect
18	Ground	Ground	No Connect	Ground	Ground	No Connect
19	Ref Clock+	Ref Clock-	No Connect	No Connect	No Connect	No Connect

XMC Bus Connector (J15) for the CPU-31-12

B. BIOS & Setup

The CPU-31-12 uses General Software's Embedded BIOS with StrongFrame™ Technology, Rev 6. The BIOS is configured with the System Setup Utility, accessible from the Preboot Menu. This photo shows the initial splash screen that is displayed after powering up the system as the BIOS runs through the Power On Self Test (POST). When your system is powered on, Embedded BIOS tests and initializes the hardware and programs the chipset and other peripheral components.



To enter the Setup mode, please press the delete key on your keyboard after powering up your system, during POST.

B.1 Redirecting to a Serial Port

Setup may be run from the main keyboard and video display or from a terminal emulator program running on a host computer connected to the system through a serial cable. To use a serial port, connect a dumb terminal or a PC running a terminal emulation utility like Hyperterminal to COM1 via a null modem. Next, set the communications parameters of the host's terminal program to 115Kbaud. Other parameters are 8-bit, no parity, and one stop bit. Do not enable XON/XOFF or hardware flow control.

With this link set up, power on the system. Press ^C a few times on your dumb terminal or your PC as the system boots. POST will redirect to the serial console, and after it has completed its early stages, it will start the preboot menu.

B.2 Setup Menus

The standard Embedded BIOS setup menus are described below in the order they generally appear in the menuing system (**Dynatem cannot vouch for support for all BIOS functions described in the subsequent sections**):

Main	Display main system components and allow editing of date and time.
Exit	Save changes and exit, discard changes and exit, or restore factory default settings.
Boot	Configure boot actions and boot devices.
POST	Configure POST.
PnP	Configure Plug-n-Play for non-ACPI OSes.

Appendix B – BIOS & Setup

SIO	Configure Super I/O devices such as serial ports and parallel ports.
Features	Enable and disable system BIOS features like ACPI, APM, PnP, MP, quick boot, and the splash screen.
Firmware	Configure Firmware Technology and the features that use it, such as USB keyboard and mouse support (commonly, USB HID), boot from USB (commonly, USB Boot), and applications such as high availability, boot security (not user security, but chain-of-trust security), and network-based remote access.
Misc	Configure miscellaneous BIOS settings that do not fall into any other category.
Shadowing	Configure chipset shadow RAM regions.
Security	Configure which BIOS features require user authentication before they perform their functions
CUI	Configure the layout and coloring of the Common User Interface (CUI) display engine that supports preboot applications.
Chipset	Configure any chipset-specific parameters, such as memory, CPU, and bus timing, and availability of chipset-specific features such as TFT support. Highly platform-specific and entirely up to the OEM's implementation.

B.3 Navigating Setup Menus and Fields

Navigation (moving your cursor around, selecting items, and changing them) is easy in the Setup system. The following chart is a helpful user reference:

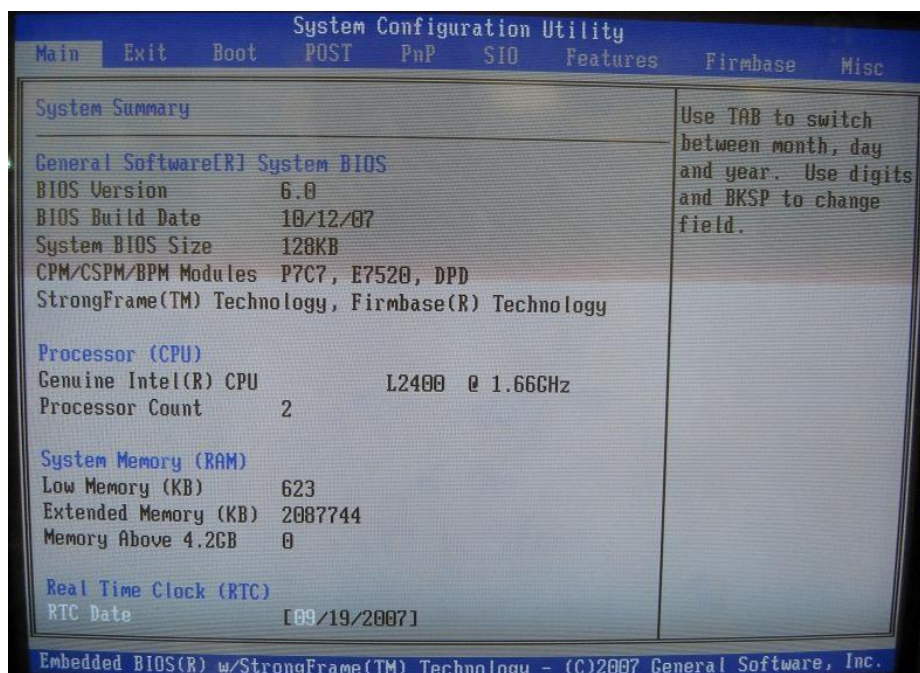
UP key (also ^E)	Move the cursor to the line above, scrolling the window as necessary.
DOWN key (also ^X)	Move the cursor to the line below, scrolling the window as necessary.
LEFT key	Go back to the menu to the left of the currently-displayed menu in the menu bar.
RIGHT key	Go forward to the menu to the right of the currently-displayed menu in the menu bar.
PGUP key	Move the cursor up several lines (a full window's worth), scrolling the window as necessary.
PGDN key	Move the cursor down several lines (a full window's worth), scrolling the window as necessary.
HOME key	Move the cursor to the first configurable field in the current menu, scrolling the window as necessary.
END key	Move the cursor to the last configurable field in the current menu, scrolling the window as necessary.
ESC key	Exit the Setup system, discarding all changes (except date/time changes, which take place on-the-fly.)
TAB key	Move the cursor down to the next configurable field.
Shift-TAB key (backtab)	Move the cursor up to the last configurable field.
+ key	Toggle an Enable/Disable field, or increase a numeric field's value.
- key	Toggle an Enable/Disable field, or decrease a numeric field's value.
SPACE key	Toggle an Enable/Disable field.
BKSP key	Reset an Enable/Disable or multiple-choice field, or back-up in numeric or string fields.
Digits (0-9)	Used to enter numeric parameters.
Alphabetic (A-Z, a-z)	Used to enter text data on ASCII fields such as email addresses.
Special symbols (!@#\$%^&* _+={}[] , etc.)	Used to enter special text on ASCII fields that permit these characters.

The basic idea when using the Setup system is to navigate to the menus containing fields you want to review, and change those fields as desired. When your settings are complete, navigate to the EXIT menu, and select “Save Settings and Restart”. This causes the settings to be stored in nonvolatile memory in the system, and the system will reboot so that POST can configure itself with the new settings.

After rebooting it may be desirable to reenter the Setup system as necessary to adjust settings as necessary. Once the system boots, the Setup system cannot be entered; this is because the memory used by the BIOS configuration manager is deallocated by the system BIOS, so that it can be used by the OS when it boots. To reenter the Setup system after boot, simply reset the system or power off and power back on.

B.4 Main Setup Menu

The first menu always showing in the Setup system is the Main menu (unless disabled by the OEM.) This menu is shown in Figure 3.1 below.



The Main menu provides a system summary about the BIOS, processor, system memory, date and time, and any other items configured by the OEM. The BIOS information is obtained by Setup from the internal system BIOS build itself; this information is useful when obtaining support for your system.

PLEASE CALL Dynatem at (800)543-3830 FOR BIOS SUPPORT; DO NOT CALL GENERAL SOFTWARE DIRECTLY.

BIOS Version	Indicates the major and minor core architecture versions (6.x, where x is a number from 0 to 999.)
BIOS Build Date	Date in MM/DD/YY format on which Dynatem built the system BIOS binary file.
System BIOS Size	Size of BIOS exposed in low memory below the 1MB boundary. Commonly, 128KB would mean that the BIOS is visible in the address space from E000:0000 to F000:FFFF.

Appendix B – BIOS & Setup

CPM/CSPM/BPM Modules	Indicates the names of the key architectural modules used to create the system BIOS binary file. The CPM module provides the CPU family support; the CSPM module provides the northbridge support; and the BPM module provides the board-level support.
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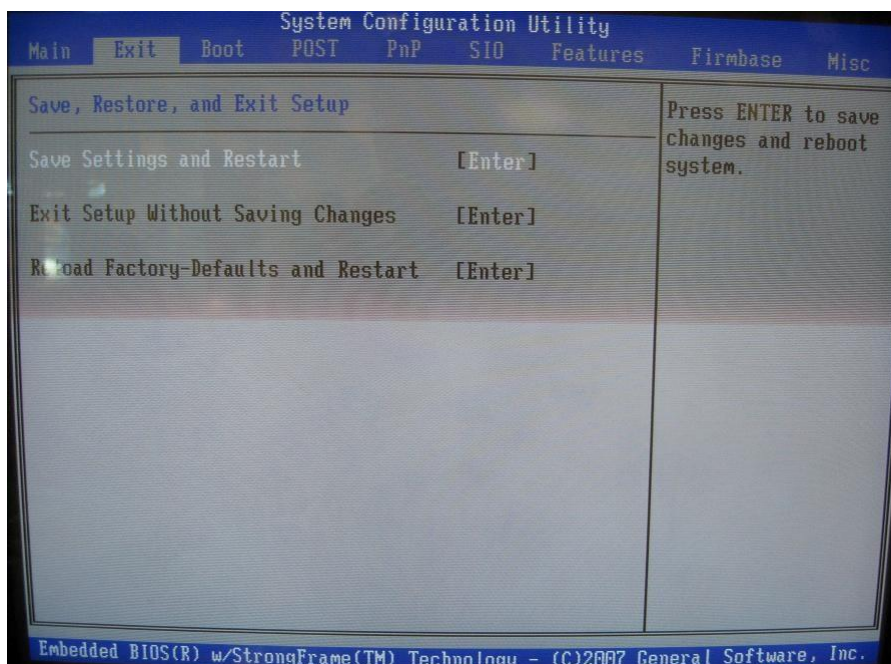
The CPU information is normally obtained by querying the Processor Brand String in the CPU's MSRs; the method used to achieve this is beyond the scope of this document.

The system memory information does not describe physical RAM; rather it describes the RAM as configured, subtracting RAM used for System Management Mode, Shadowing, Video buffers, and other uses. This provides realistic values about how much memory is actually available to operating systems and applications.

The Real Time Clock fields are editable with keystrokes. To navigate through the MM/DD/YYYY and HH:MM:SS fields, use the TAB and BACKTAB keys. The hours are normally specified in military time; thus 13 means 1pm, or one hour after noon, whereas 01 means 1am, or one hour after midnight. When the cursor leaves RTC fields, they either affect the battery-backed RTC right away, allowing the system to continue with your new settings, or they revert back to old values if the new values are not valid entries.

B.5 Exit Setup Menu

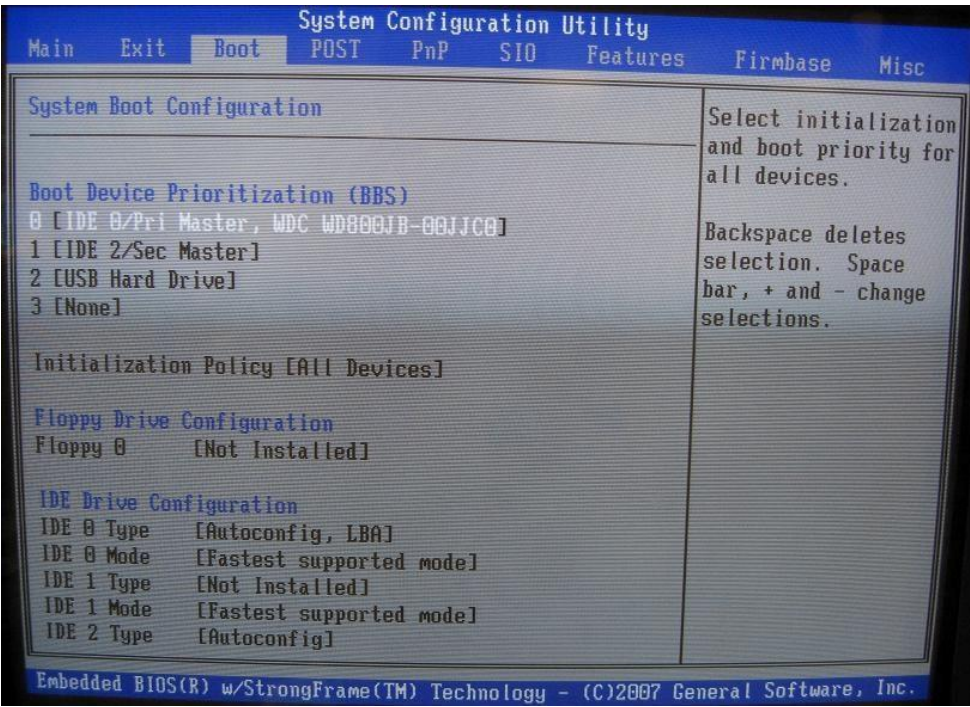
The Exit menu provides methods for saving changes made in other menus, discarding changes, or reloading the standard system settings. This menu is shown in Figure 3.2 below.



To select any of these options, position the cursor over the option and press the ENTER key. Pressing the ESC key at any time within the Setup system is equivalent to requesting "Exit Setup Without Saving Changes."

B.6 Boot Setup Menu

The Boot menu allows the system's boot actions and boot devices to be configured. This menu is shown here:



The BBS portion of this menu lists the devices and activities to be performed in the order in which they appear in the list. When the BIOS completes POST, it follows this list, attempting to process each item. Some items are drives, such as an ATA/IDE drive, or a USB hard disk, or CDROM.

The ordering of the drives in the BBS list controls the BIOS in several ways. First, it is the list of drives that is scanned and assigned BIOS unit numbers for DOS (for example 80h, 81h, 83h, and so on for hard drives). If a drive on the list is not plugged in or working properly, the BIOS moves on to the next drive, skipping the inoperative one.

Second, once the drives in the list have been verified, POST attempts to boot from them in that order as well. Drives without bootable partitions might be configured, but skipped over in the boot phase, so that other drives on the list become candidates for booting the OS.

The BBS list also contains other boot actions, such as boot from network cards and PCI slots, as well as special BIOS boot actions like “Boot EFI”, “Boot Windows CE”, or even “Boot Debugger”. When deciding what boot action to do first and then next in succession, POST first scans all the drives in the list to verify they are present and operating properly (as described earlier in this section) and then goes down the list and tries to perform the actions in order. During this boot phase, if the list item is a drive, an attempt is made to boot from the boot record of that drive. If the list item is a device like a network card or PCI slot, an attempt is made to boot from that device. If the list item is a software item like “Boot Debugger”, then it performs that action, and when that action completes, it moves on to the next item in the BBS list.

The table that follows lists the set of standard boot action items:

“drive name” – The system BIOS may list the drive’s name in a generic sense (i.e., “USB Hard Drive”) if the drive has not been detected yet, or the drive’s full manufacturing name and serial number (if detected.)	Boot from the MBR/PBR of the named BIOSaware IPL drive (BAID). The drive may be Legacy Floppy, PATA, SATA, Compact Flash, or a USB drive.
IDE0/Primary Master Primary	Master PATA drive or SATA mapping by the chipset, routed to the backplane via J5.

Appendix B – BIOS & Setup

IDE1/Primary Slave	Primary Slave PATA drive or SATA mapping by the chipset, routed to the backplane via J5.
IDE2/Secondary Master	Secondary Master PATA drive or SATA mapping by the chipset, routed to on-board CompactFlash
IDE CDROM	First detected IDE CDROM.
USB Floppy Drive	First detected USB floppy drive.
USB Hard Drive	First detected USB hard drive.
USB CDROM Drive	First detected USB CDROM.
Enter Board Information Browser	Invoke HTML Browser on 0.HTM in ROM.
Enter BIOS Setup Screen	Invoke System Setup Utility in ROM.
Enter BIOS Debugger	Invoke BIOS debugger in ROM.
Reboot System	Restart system.
Power Off System	Invoke S5 state, powering off system.
PCI Slot [n]	Boot from device in PCI Slot 'n'.
Network	Boot from any network adapter.
SCSI	Boot from external SCSI device (on PMC/XMC card).
Boot EFI Binary	Boot EFI kernel from ROM or disk, depending on the EFI source setting in the Features menu. If disk is selected, then the BIOS searches all the configured disks in the system in the order they appear in the BBS list, attempting to load EFILDR.BIN from the root directory in the FAT file system located on those drives.
Boot Windows CE Image	Boot Windows CE kernel from disk. The BIOS searches all the configured disks in the system in the order they appear in the BBS list, attempting to load NK.BIN from the root directory in the FAT file system located on those drives.
Boot Graphical Desktop	Boot Firmbase GUI supporting graphical Firmbase applications as well as booting DOS in a graphical window. For applications requiring instant-on functionality even when the OS is not available or is still loading.

The photograph above shows a common setup of the BBS list for desktop applications. In this example, the first boot device is the Western Digital IDE hard drive (WDC WD800JB-00JJC0) connected to the target as a Primary Master IDE drive. The second boot device is the Secondary Master and this is the on-board CompactFlash. The third device is a USB Hard Drive. A fourth boot device, "None", is a placeholder that is simply used to add more entries in the setup screen; "None" is not actually executed by POST as a boot action item.

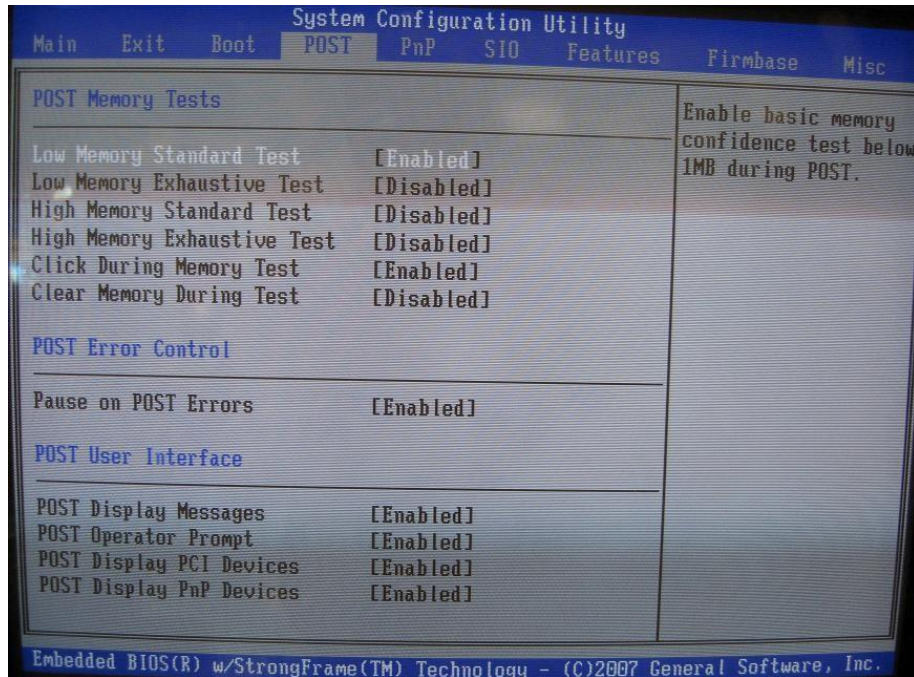
In addition to the BBS boot device list, there are two more sections in the BOOT menu; namely, the Floppy Drive Configuration and IDE Drive Configuration sections. Both of these sections tell the BIOS what kind of equipment is connected to the motherboard but the floppy drive interface has not been implemented so please ignore this and leave it as "Not Installed". Similarly, the IDE Drive Configuration section describes the type of hard drive equipment that is connected to the motherboard, including the cable type. IDE drives, or actually more properly Parallel ATA (PATA) drives, are connected to the motherboard with a flat cable with either 40 or 80 wires running in parallel (hence, Parallel ATA, as opposed to Serial ATA.) The 40-pin connector supports speeds up to UDMA2, whereas 80-pin cables are needed for higher transfer rates to eliminate noise. The BIOS can be told what type of cable is available, so that it knows whether higher transfer rates are allowed; or, it can be told to autodetect the cable type, in which case the drive and the motherboard must both support the hardware protocol used to autodetect the drive's cable type.

Note: PATA cable autodetection sometimes fails with older drives, so 40-pin is the default, to ensure data integrity.

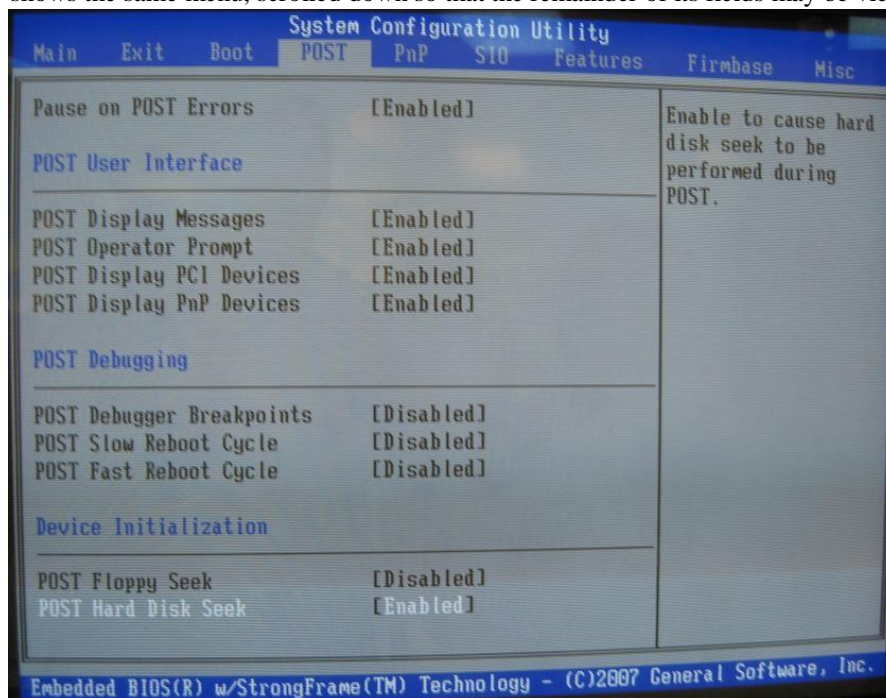
For higher performance, you should change this setting to 80-pin or AUTO if an 80-pin cable is installed.

B.7 POST Setup Menu

The POST menu is used to configure POST. This menu is shown in the following figure (scrolled down more so the full set of options can be seen.) Be sure to review the Features menu, where additional items can be configured, such as the Splash Screen and BIOS initiatives.



The figure below shows the same menu, scrolled down so that the remainder of its fields may be viewed.



Appendix B – BIOS & Setup

The following table describes the settings associated with the POST setup menu's Memory Test section.

Low Memory Standard Test	Enable basic memory confidence test, of memory below 1MB address boundary (conventional memory, or memory normally used by DOS.)
Low Memory Exhaustive Test	Enable exhaustive memory confidence test of memory below 1MB address boundary.
High Memory Standard Test	Enable basic memory confidence test, of memory between 1MB and 4.2GB address boundaries (extended memory.)
High Memory Exhaustive Test	Enable exhaustive memory confidence test, of memory between 1MB and 4.2GB address boundaries.
Huge Memory Standard Test	Enable basic memory confidence test, of memory above 4.2GB address boundary (available using PAE technology.)
Huge Memory Exhaustive Test	Enable exhaustive memory confidence test, of memory above 4.2GB address boundary.
Click During Memory Test	Enable/disable speaker click when testing each block.
Clear Memory During Test	Enable storing 0's in all memory locations tested. Only necessary when some legacy DOS programs are run, as they may rely on cleared memory to operate properly.

The following table describes the settings associated with the POST setup menu's Error Control section:

Pause on POST Errors	Enable pause when errors are detected during POST, so that the user can view the error message and enter Setup or continue to boot the OS.
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The following table describes the settings associated with the POST setup menu's POST User Interface section:

POST Display Messages	Enable display of text messages during POST. When disabled, POST is "quiet."
POST Operator Prompt	Enable operator prompts if POST is configured to ask interactive questions of the user about whether to load specific features; i.e., whether or not to load SMM.
POST Display PCI Devices	Enable display of PCI devices.
POST Display PnP Devices	Enable display of ISA PnP devices.

The following table describes the settings associated with the POST setup menu's Debugging section:

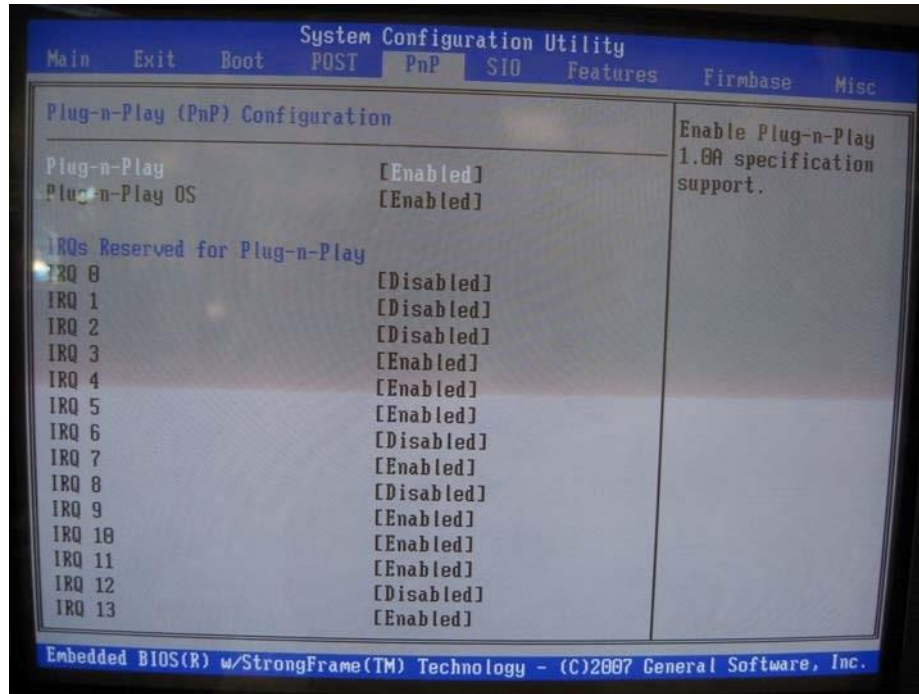
POST Debugger Breakpoints	Enable processing of INT 3 (breakpoint) instructions embedded into option ROMs. When enabled, if an INT 3 instruction is encountered, control is transferred to the BIOS debugger, so that the option ROM can be debugged. When disabled, these instructions perform no action.
POST Fast Reboot Cycle	Enable early reboot in POST, allowing service technician to verify that the hardware can reboot very quickly many times in succession. Platform will continue to reboot after every boot until the system's CMOS is reset, as there is no way to enter Setup from this early point during POST.
POST Slow Reboot Cycle	Enable late reboot in POST, allowing service technician to cause the system to move through POST and then reboot, causing POST to be reexecuted, over and over, until Setup is reentered and this option is disabled. When left unattended, this is a straightforward way of having POST exercise system memory and peripherals without requiring a boot to a drive with an operating system installed.

The following table describes the settings associated with the POST setup menu's Device Initialization section:

POST Floppy Seek	Enable head seek on each floppy drive configured in the system. Used to recalibrate the drive in some systems with older DOS operating systems.
POST Hard Disk Seek	Enable head seek on each hard drive configured in the system. This is a way of extending the standard testing performed on each drive during POST, by requesting that the drive actually move the head. Not available with all drives.

B.8 PnP Setup Menu

The PnP menu is used to configure Plug-n-Play, a legacy BIOS initiative used to support operating systems such as Windows95, Windows98, and WindowsNT. ACPI has largely replaced this feature; however, it is necessary for platforms to support older operating systems.



The PnP menu consists of two sections; basic configuration that enables Plug-n-Play and identifies if a PnP should perform configuration or let the OS do it; and then, another section that defines which system IRQs should be reserved for PnP's use, so that PCI doesn't use them. The following table presents the fields in the PnP menu.

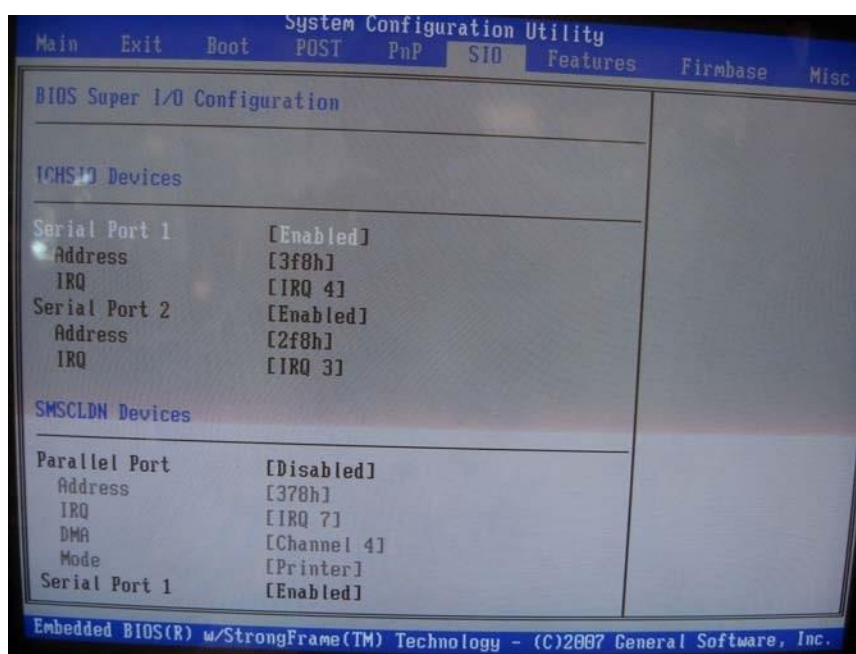
Plug-n-Play	Enable PnP feature. When disabled, a PnPaware OS will not find any PnP services in the BIOS, and all other configuration parameters in the menu will be greyed out. Enable to support legacy OSes like DOS, Windows95, Windows98, and WindowsNT. Disable for operating systems like WindowsXP or Windows Vista, or for Linux operating systems with ACPI support.
Plug-n-Play OS	Enable delay of configuration of PnP hardware and option ROMs. When enabled, BIOS will NOT configure the devices, and instead defer assignment of resources, such as DMA, I/O, memory, and IRQs, to the PnP OS. When disabled, the BIOS performs conflict detection and resolution, and assigns resources for the OS. Disable this parameter when running non-PnP OSes like DOS. Enable this parameter when running PnP OSes like Windows95, Windows98, and WindowsNT.
IRQ0	Enable exclusive use of IRQ0 by PnP.
IRQ1	Enable exclusive use of IRQ1 by PnP.
IRQ2	Enable exclusive use of IRQ2 by PnP.
IRQ3	Enable exclusive use of IRQ3 by PnP.
IRQ4	Enable exclusive use of IRQ4 by PnP.
IRQ5	Enable exclusive use of IRQ5 by PnP.
IRQ6	Enable exclusive use of IRQ6 by PnP.
IRQ7	Enable exclusive use of IRQ7 by PnP.
IRQ8	Enable exclusive use of IRQ8 by PnP.

Appendix B – BIOS & Setup

IRQ9	Enable exclusive use of IRQ9 by PnP.
IRQ10	Enable exclusive use of IRQ10 by PnP.
IRQ11	Enable exclusive use of IRQ11 by PnP.
IRQ12	Enable exclusive use of IRQ12 by PnP.
IRQ13	Enable exclusive use of IRQ13 by PnP.
IRQ14	Enable exclusive use of IRQ14 by PnP.
IRQ15	Enable exclusive use of IRQ15 by PnP.

B.9 Super I/O (SIO) Setup Menu

The SIO menu is used to configure the LPC47B27x Super I/O device. The only implemented I/O on this chip are the PS/2 mouse and keyboard and two 2-wire COM ports (COM3 & COM4). Basically this window is used to configure COM3 & COM4 (though they are referred to as Serial Ports 1 & 2 in the SIO Setup Menu):



POST reads these settings in the menu shown above and programs the Super I/O part accordingly, enabling and disabling devices as requested. The disabled devices are not further programmed, since they are actually disabled in hardware. In the figure above, legacy I/O addresses and IRQs are as follows:

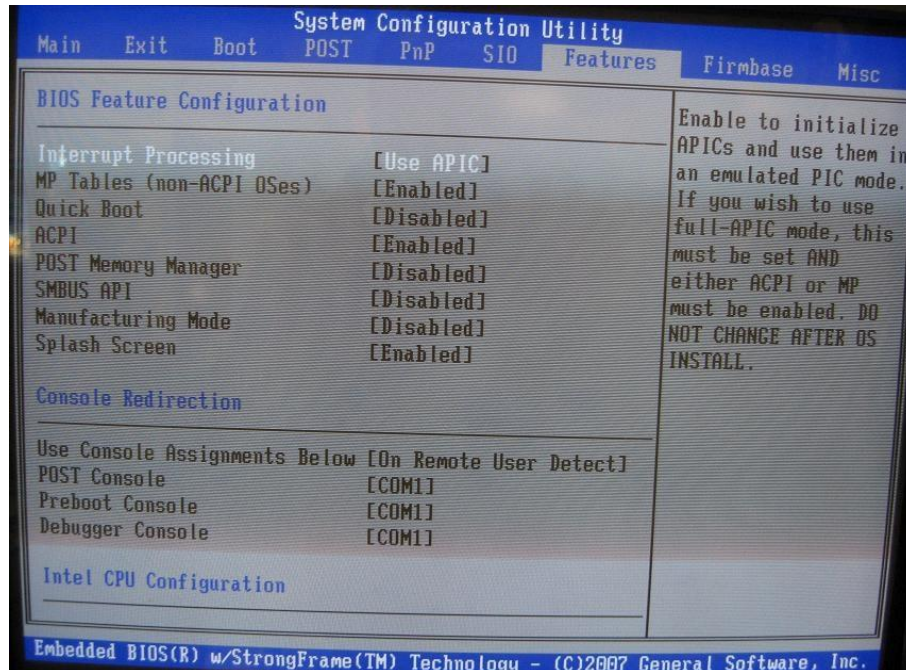
COM3 – I/O 3f8h, IRQ4.

COM4 – I/O 2f8h, IRQ3.

It should be noted that these are not the only possible addresses, but they are the ones that will ensure compatibility with the most legacy software, especially early DOS programs that do not use BIOS to access the COM ports.

B.10 Features Setup Menu

The Features menu is used to configure the system BIOS' major features, including Quick Boot, APM, ACPI, PMM, SMBUS, SMBIOS, Manufacturing Mode, Splash Screen, Console Redirection, and others added by the OEM. This figure shows a typical Features Setup menu.



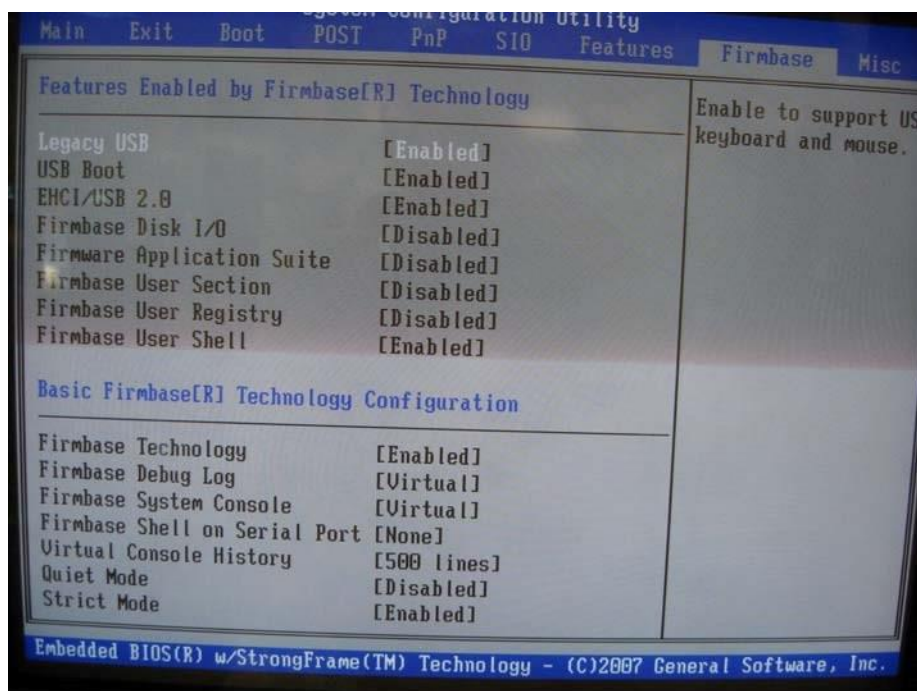
The following table describes each setting in the Features menu :

Quick Boot	Enable time-optimized POST, causing certain preconfigured OEM optimizations to be made when the system boots. Depending on the system, Quick Boot can reach the DOS prompt in as little as 85ms (milliseconds.)
Advanced Power Management (APM)	Enable legacy power management, used by the system when an ACPI-aware operating system is not running (during POST, such as when the system is running the preboot environment, or while running DOS, Windows95, Windows98, or Linux kernels below version 2.6.) Uses the SMM feature (see Firmware) to operate properly.
ACPI	Enable ACPI system description and power management (ACPI replaces PnP and APM.) Used with ACPI-aware OSes such as Linux kernels version 2.6 and above, Windows XP, and Windows Vista. Commonly also uses the SMM feature (see Firmware) to operate properly.
POST Memory Manager (PMM)	Enable memory allocation services for option ROMs, especially network cards running PXE. Some option ROMs may use this interface incorrectly, causing system crashes. Other PXE option ROMs may not run if PXE is not supported. Because of the state of these option ROMs, the setting is provided as an option to the user.
SMBUS API	Enable INT 15h services that permit certain software to access devices on the system's SMBUS without having knowledge of the SMBUS controller itself.
System Management BIOS (SMBIOS)	Enable System Management BIOS interface specification support, exposing information about the type of hardware, including the chassis, motherboard layout, type of CPU and DRAM sticks, to applications such as WfM, which runs on PXE in the preboot environment.
Manufacturing Mode	Enable automatic entry into manufacturing mode when POST encounters a critical error. Used in closed device settings such as smart phones that need access to docking stations when they don't boot. Leave disabled.
Splash Screen	Enable graphical POST

Console Redirection	Configure the console redirection feature over a serial port. Automatic – causes POST, the debugger, and the preboot environment to use the system's first serial port (COM1) when an RS232 cable is detected with DSR and CTS modem signals active, indicating a terminal emulation program is likely to be attached to the other end of the cable. Always – causes the BIOS to always use the serial port as the console, without testing for the presence of the terminal emulation program. Never – causes the BIOS to never invoke console redirection, but instead always use the main keyboard and video display. If there is no keyboard or video display, the system operates headless.
EFI Source	Configure the location (ROM or disk) where the EFI boot action can find the EFILDR.BIN image. An image may be merged with the system BIOS into the system ROM, or it may be placed in the root directory of any bootable mass storage device.

B.11 Firmware Setup Menu

The Firmware menu configures the Firmware Technology component of the system BIOS, including all of the features enabled by it; i.e., legacy USB keyboard and mouse, boot from USB devices, and support of Firmware applications such as Boot Security, Platform Update Facility, and High Availability Monitor. This menu has several parts, with the most basic user oriented feature options in the top section, and the more technical tuning parameters located in the lower sections.



The following table presents the settings that enable high-level features enabled by Firmware Technology:

Legacy USB	Enables BIOS support for USB keyboards and mice. Up to 8 USB keyboards and 8 USB mice may be supported at a time. Use of PS/2 keyboard and mouse concurrently with USB devices is discouraged, as the legacy PS/2 keyboard controller cannot easily separate simultaneous data streams from both device classes.
USB Boot	Enables BIOS support for accessing USB mass storage devices and emulating legacy floppy, hard drive, and CDROM drive devices with them. Enable this option in order for USB devices to be supported in the BBS device list(see the BOOT menu.)

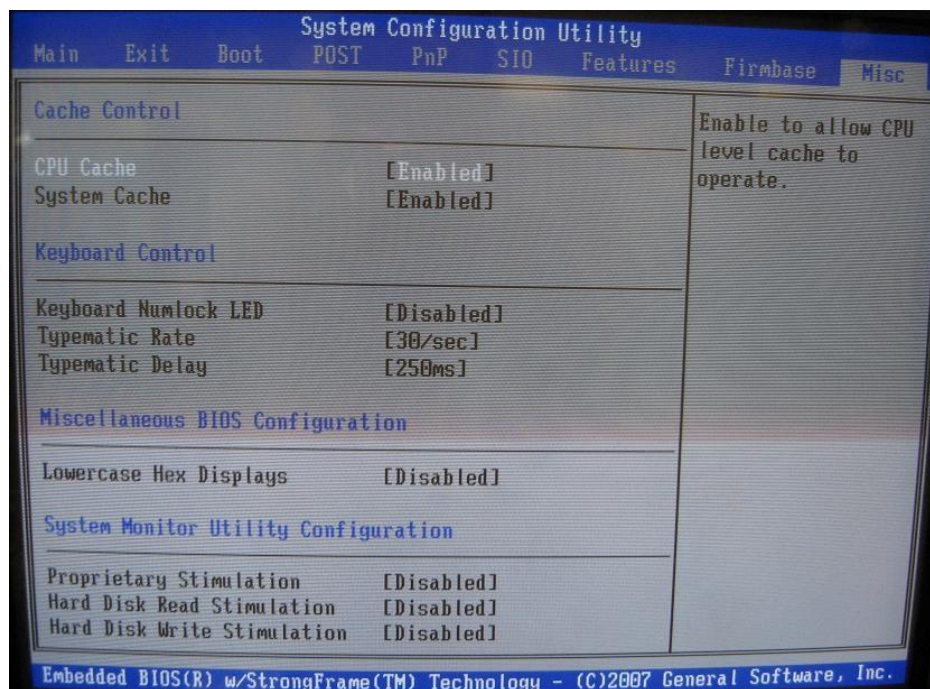
EHCI/USB 2.0	Enables EHCI Firmware Technology driver, allowing USB Boot feature to use high speed transfers on USB 2.0 ports in the system.
Firmware Disk I/O	Enables Firmware Technology FAT file system driver, so that Firmware applications such as Boot Security, Platform Update Facility, and HA Monitor, as well as the HA and TCB components of the kernel, have access to files residing on drives containing FAT file systems. Also turn on this option if you wish to run Firmware applications from FAT file systems on either ATA or USB mass storage devices.
Firmware Application Suite	Enables Firmware applications configured for the system by the OEM. Typically includes Boot Security, Platform Update Facility, and High Availability Monitor.
Firmware User Registry	Not used.
Firmware User Shell	Enables Firmware Technology command line interpreter, a multi-user command shell with DOS-like and Unix-like command structure; can be used to start Firmware applications written with the Firmware SDK, a General Software product.
Firmware Technology	Enables Firmware Technology as a whole, the industry's most comprehensive and full-featured System Management Mode (SMM) operating environment. Some hardware platforms require Firmware Technology to run, as they may use it to virtualize hardware such as virtual video and audio PCI devices. Some BIOS features, such as ACPI and APM, may require Firmware Technology to operate.
Firmware Debug Log	<p>Specifies the device used by Firmware Technology components (kernel, drivers, and programs) to display debugging instrumentation produced with the dprintf and DPRINTF system functions.</p> <p>None – Instrumentation disabled. COM1 – Write text to 1st serial port. COM2 – Write text to 2nd serial port. COM3 – Write text to 3rd serial port. COM4 – Write text to 4th serial port. Virtual – Write text to virtual console</p> <p>If enabled, this console can provide diagnostic messages (similar to the types displayed by Linux when it boots) for Firmware Technology features such as USB HID and USB Boot.</p>
Firmware System Console	<p>Specifies the device used by Firmware Technology's system process when it initializes the kernel and processes the [SYSTEM] registry section, including its Start and Run commands.</p> <p>None – System console disabled. COM1 – Write text to 1st serial port. COM2 – Write text to 2nd serial port. COM3 – Write text to 3rd serial port. COM4 – Write text to 4th serial port. Virtual – Write text to virtual console</p> <p>If enabled, this console can provide a list of sign-on banners of all Firmware applications loaded during system initialization.</p>

Appendix B – BIOS & Setup

Firmware Shell on Serial Port	<p>Specifies a serial port that may be used by Firmware Technology's command line interpreter as an extra user session for systems that do not have a keyboard or monitor to support virtual consoles.</p> <p>None – Serial console disabled. COM1 – Console on 1st serial port. COM2 – Console on 2nd serial port. COM3 – Console on 3rd serial port. COM4 – Console on 4th serial port.</p>
Virtual Console History	<p>Specifies the number of lines of text that Firmware Technology maintains in its virtual console feature, allowing the user to scrollback through lines previously displayed and scrolled off the screen. OEMs may configure a set of values, such as 20, 50, 100, 200, and 500 lines.</p>
Quiet Mode	<p>Enables a feature that causes the Firmware kernel to suppress its standard messages to the system console.</p>
Strict Mode	<p>Enables a feature that causes the Firmware kernel to abort any processes in the system that make software errors in calling system API functions. Examples include blocking at IRQs other than IRQ_THREAD, or passing a NULL pointer to a C library function that requires a non-NULL pointer, etc.</p> <p>Disabling this feature causes the kernel to skip over the activity that discovered the programming error in the application, allowing it to continue if at all possible, with the consequence that the program may not operate correctly.</p>

B.12 Miscellaneous Setup Menu

The Misc menu provides for configuration of BIOS settings that don't easily fit in any other category. They include Cache Control, Keyboard Control, Debugger Settings, and System Monitor Utility Configuration parameters.



The following table presents the settings in the Misc Setup menu:

System Cache	Enables POST's support for cache in the system. Modern processors virtually require cache to be enabled to achieve acceptable performance. However, to diagnose certain problems related to caching in the system, such as multiprocessing systems, it may be desirable to disable this setting.
Keyboard Numlock LED	Enables the Numlock key when POST initializes the PS/2 keyboard.
Typematic Rate	Specify the rate at which the PS/2 keyboard controller repeats characters when most keys are pressed down. USB typematic is automatic and does not use this parameter.
Typematic Delay	Specifies the amount of time a repeating key may be pressed on a PS/2 keyboard until the key repeat feature begins repeating the keystroke. USB typematic is automatic and does not use this parameter.
Lowercase Hex Displays	Enables the display of hexadecimal numbers in the debugger with lowercase letters instead of uppercase letters (ie, 2f8ah instead of 2F8AH.)
Proprietary Stimulation	Enables System Monitor's callout to the OEM's BPM adaptation code to execute code that causes stimulation of the SMM environment for measurement purposes.
Hard Disk Read Stimulation	Enables System Monitor's read of a preconfigured number of sectors from a location on the first hard disk in the system in order to stimulate the SMM environment. This is useful when measuring code path lengths in USB boot, when the first hard drive is configured in the BBS list as a USB hard drive.
Hard Disk Write Stimulation	<p>Enables System Monitor's write of a preconfigured number of sectors to a location on the first hard disk in the system in order to stimulate the SMM environment. This is useful when measuring code path lengths in USB boot, when the first hard drive is configured in the BBS list as a USB hard drive.</p> <p>Please note that when this parameter is selected, the system automatically enables reading, so that the stimulation of the system includes reading a range of sectors into a memory buffer, and writing the same data back to the same range of sectors for safety. Thus, this feature is theoretically nondestructive.</p> <p>WARNING: YOU ARE ADVISED THAT THIS FEATURE COULD CAUSE DATA LOSS AT YOUR SOLE EXPENSE; ACCORDINGLY, IT IS PROVIDED AS-IS WITHOUT WARRANTY OF ANY KIND. ALWAYS BACKUP YOUR DATA BEFORE PERFORMING DIAGNOSTICS ON ANY SYSTEM, AS THEY COULD CAUSE DATA LOSS.</p>
Floppy Disk Read Stimulation	There is no Floppy Drive interface implemented on the CPU-31-12.

C. Power and Environmental Requirements

The CPU-31-12 power and environmental requirements are shown in the tables below.

Condition	Power Requirements
1.5 GHz Core 2 Duo	+5 VDC @ 5.5 Amps, peak 3.3 VDC @ 2.0 Amps, steady 3.0 VDC Lithium Coin Cell @ 3.4 μ A
2.16 GHz Core 2 Duo	+5 VDC @ 8.0 Amps, peak 3.3 VDC @ 2.0 Amps, steady 3.0 VDC Lithium Coin Cell @ 3.4 μ A

Power Requirements

The 3 Volt lithium coin cell is a CR2032 with 190 mAh capacity and it is used to battery-back the Real Time Clock, the 2 MB of NV-SRAM, and the BIOS's NV-RAM. At 3.4 μ A this battery should last for over six years with power off.

Condition	Environmental Requirements
Operating Temperature	-20 to 85 $^{\circ}$ C with Thermal Monitor II enabled
Storage Temperature	-50 $^{\circ}$ to +105 $^{\circ}$ C

Environmental Requirements

Appendix C – Power & Environment Requirements

D. XPDDRIO Rear Plug-in I/O Expansion Module for the CPU-31-12

Dynattem offers a rear plug-in paddle card for I/O expansion with the CPU-31-12. Essentially the CPU-31-12 RT00 routes the

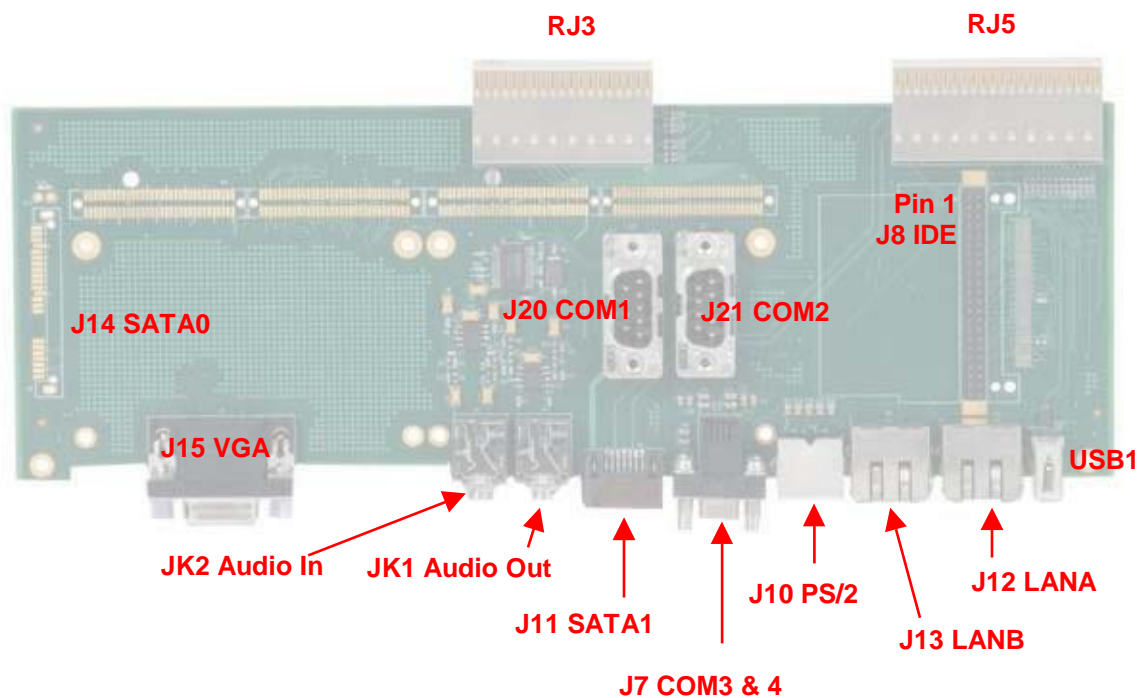
CPU-31-12's backplane I/O, including IDE, COM1/2/3/4, P/S2 Mouse/Keyboard interfaces, VGA, a USB port, and two SATA ports (one supporting an on-board hard drive) to industry standard connectors. A USB port is routed to a sound chip to support Audio In and Audio Out.

The two Ethernet ports and PMC Site #2 I/O are routed through RJ3. IDE, the four COM ports, two USB ports (one routed to a sound chip), two SATA ports, and the VGA port and mouse and keyboard ports are routed through RJ5.

Two Serial ATA ports are routed through RJ3. The XPDDRIO also routes two PICMG 2.16 compliant 1 Gb Ethernet ports from RJ3 to two industry standard connectors for situations where PICMG 2.16 backplane fabric switching is not used.

The Super I/O device used for COM3/4, P/S2 Mouse/Keyboard, LPT1, and FDC is SMSC's LPC47B272 and a data sheet can be found at: <http://www.smsc.com/main/catalog/lpc47b27x.html>

Here is a photograph of the XPDDRIO with the connectors indicated:



D.1 XPDDRIO Connector Pinouts

All four com ports are set up for RS-232 operation. J7 is a stacked Micro D-subminiature connector that supports COM3 & COM4. The pinouts of the four connectors are identical:

Pin	RS-232 Signals
1	Data Carrier Detect (DCD) Input
2	Received Data (RxD) Input
3	Transmitted Data (TxD) Output
4	Data Terminal Ready (DTR) Output
5	GND
6	Data Set Ready (DSR) Input
7	Request To Send (RTS) Output
8	Clear To Send (CTS) Input
9	Ring Indicator (RI) Input

COM Connectors – DB9M Connectors J7, J20, and J21. The metal shell of the connector goes to chassis ground.

Pin	Signal	Pin	Signal
1	RST#	2	GND
3	D7	4	D8
5	D6	6	D9
7	D5	8	D10
9	D4	10	D11
11	D3	12	D12
13	D2	14	D13
15	D1	16	D14
17	D0	18	D15
19	GND	20	No connection
21	DMARQ0	22	GND
23	IOW#	24	GND
25	IOR#	26	GND
27	IORDY	28	470-ohm pull-down
29	DMAACK0	30	GND

31	IRQ14	32	No connection
33	DA1	34	No connection
35	DA0	36	DA2
37	CS1Fx	38	CS3Fx
39	LED Control	40	GND

Primary IDE Interface Connector (J8) – 40-pin Dual-row 0.1” Header

Appendix D – XPDDRIO Rear Plug-in I/O Expansion Module for the CPU-31-12

J10 combines the PS/2 Mouse and Keyboard interfaces on one connector. A Y-splitter cable is required to separate them.

Pin	Signal Description
1	Keyboard Data
2	Mouse Data
3	GND
4	+5 VDC (via 1 amp self-resetting fuse F1)
5	Keyboard Clock
6	Mouse Clock

Keyboard/Mouse Connector (J10) –Mini-DIN Receptacle. The metal shell of the connector goes to chassis ground.

J11 (SATA1) is a Serial ATA connector that has the following pinout:

Pin	Signal
1	GND
2	A+
3	A-
4	GND
5	B-
6	B+
7	GND

Serial ATA Connectors (J11) Pinout

Appendix D – XPDDRIO Rear Plug-in I/O Expansion Module for the CPU-31-12

The XPDDRIO uses two RJ45 connectors to provide two 1 Gb Ethernet ports. These lines are routed through 0 ohm resistors R25 – R44. These ports are also routed to the RJ3 connector in compliance with PICMG 2.16. Leave the resistors off in systems that utilize PICMG 2.16 backplane networking.

J12		
Pin	10/100 Signal Description	Gb Signal Description
A1	Port A Transmit Data + (TX+)	TJ3+
A2	A Transmit Data - (TX-)	TJ3-
A3	A Receive Data + (RX+)	TP1+
A4	Unused	TJ5+
A5	Unused	TJ5-
A6	A Receive Data - (RX-)	TP1-
A7	Unused	TP3+
A8	Unused	TP3-
J13		
Pin	10/100 Signal Description	Gb Signal Description
B1	Port B Transmit Data + (TX+)	TJ3+
B2	B Transmit Data - (TX-)	TJ3-
B3	B Receive Data + (RX+)	TP1+
B4	Unused	TJ5+
B5	Unused	TJ5-
B6	B Receive Data - (RX-)	TP1-
B7	Unused	TP3+
B8	Unused	TP3-

10BaseT/100BaseTX Fast Ethernet Connector (J12/J13) – RJ45 Connectors. The metal shell of the connectors go to chassis ground.